type 3rd regions, resp., by heat treatment using the **Si** film in the contact holes as diffusion sources, especially in preparation of bipolar or bipolar complementary MOS semiconductor devices containing **npn** and **pnp transistors**. Concentrate profile in the emitter region is made easy by double diffusion, and processing step is decreased.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(formation of emitter regions by double diffusion in preparation of bipolar complementary MOS transistors)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 10 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:215560 HCAPLUS
DN 126:219448
TI Manufacture of **NPN** and **vertical PNP transistors** on same semiconductor substrates
IN Nemoto, Kyoshi
PA Olympus Optical Co, Japan
SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 09027551	A2	19970128	JP 1995-197914	19950712
PRAI JP 1995-197914		19950712		

AB The emitters of the **vertical PNP transistors** comprise the shallow and highly-concentrated P-type diffusion layers and highly-doped (with, e.g., B) poly-**Si** layers on the diffusion layers.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(doped; manufacture of **NPN** and **vertical PNP transistors** with emitters from)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 11 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1996:714579 HCAPLUS
DN 126:40582
TI The ideal **NPN vertical** BIMOS **transistor**: Analytical model, simulation and experimental results of the collector current
AU Galy, P. H.; Berland, V.
CS Pole Universitaire Leonard de Vinci, Paris, F-92916, Fr.
SO International Journal of Electronics (1996), 81(5), 501-516

CODEN: IJELA2; ISSN: 0020-7217
PB Taylor & Francis
DT Journal
LA English
AB Combining a **NPN silicon** bipolar **transistor** with a MOSFET leads to a high collector current in the hybrid mode. As this transistor has already been qual. described and as simulation was previously presented, this paper emphasizes the theor. study of the collector current, Ic, when the transistor works in the hybrid mode. A model is proposed to demonstrate the great influence of the gate bias and to confirm the previous simulation results. Exptl. results were performed with a surface **PNP** BIMOS **transistor** sample: they confirm the anal. expression of the collector current in the hybrid mode.

L19 ANSWER 12 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:497578 HCAPLUS
DN 121:97578
TI Integrated circuits
IN Imoto, Shinya
PA Rohm KK, Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 06021367	A2	19940128	JP 1992-173340	19920630
PRAI JP 1992-173340		19920630		

AB In an integrated circuit comprising a **vertical npn transistor** and a **vertical pnp transistor** on the same p-type **Si** substrate, the impurity concns. of various buried layers are such that the performance of the **vertical pnp transistor** is improved without reducing the performance of other elements.

L19 ANSWER 13 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1993:92512 HCAPLUS
DN 118:92512
TI Semiconductive integrated circuits
IN Kimura, Takashi
PA Toshiba Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 04196353	A2	19920716	JP 1990-322643	19901128
PRAI JP 1990-322643		19901128		

AB The circuit comprises (1) a 1st insulator layer formed on a semiconductor substrate, (2) an n-**Si** layer, a p-**Si** layer, and a 2nd insulator layer separating the n-**Si** and p-**Si** layers formed, (3) a **vertical npn-transistor** formed on the n-**Si** layer, and (4) a **vertical pnp-transistor** formed on the p-**Si** layer. The integrated arrangement provides a high-speed and low power consuming device.

L19 ANSWER 14 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1987:26626 HCAPLUS
DN 106:26626
TI Semiconductor device, notably a bipolar integrated circuit, comprising **npn transistors** and lateral and **vertical** **pnp transistors**
IN Ueki, Yoshio
PA Sony Corp., Japan
SO Fr. Demande, 13 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	FR 2572850	A1	19860509	FR 1985-16362	19851105
	FR 2572850	B1	19880909		
	JP 06038476	B4	19940518	JP 1984-232870	19841105
	NL 8503033	A	19860602	NL 1985-3033	19851105
	NL 194711	B	20020801		
	NL 194711	C	20021203		
	AT 8503189	A	19920315	AT 1985-3189	19851105
	AT 395272	B	19921110		
	DE 3539208	C2	19980409	DE 1985-3539208	19851105
PRAI	JP 1984-232870	A	19841105		

AB In a semiconductor device (e.g., bipolar integrated circuit) comprising n-p-n **transistors** and lateral and **vertical** p-n-p **transistors**, an n-p-n transistor is made in an n-type epitaxial layer (A) (e.g., **Si**) on a semiconductor support. The p-n-p transistor is made in an n-type semiconductor region (B) made in an n-type epitaxial layer. B Has an impurity concentration (1016-1017 cm-3) greater than that of A.

L19 ANSWER 15 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1986:434037 HCAPLUS
DN 105:34037
TI Integrated injection logic semiconductor circuit
IN Nakagawa, Shoichi
PA Matsushita Electronics Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 61048968	A2	19860310	JP 1984-170693	19840816
PRAI	JP 1984-170693		19840816		

AB An integrated injection logic semiconductor circuit is described, which consists of a lateral **pnp transistor** (injector) and reverse **vertical npn transistor** (inverter) in an n-type epitaxial layer formed on a p-type **Si** substrate via an n+-type buried layer. The n-type impurity concentration of the base region near the injector emitter is higher than that of the epitaxial layer to decrease collector-base reverse injection current.
IT **7440-21-3**, uses and miscellaneous
RL: USES (Uses)

(circuits, integrated injection logic)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 16 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1986:100695 HCAPLUS
DN 104:100695
TI Substrate injection logic operator structure
IN Depey, Maurice
PA Thomson-CSF S. A., Fr.
SO U.S., 8 pp. Cont. of U.S. Ser. No. 261,935, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4550491	A	19851105	US 1984-677885	19841203
	FR 2482368	A1	19811113	FR 1980-10566	19800512
	FR 2482368	B1	19840914		
PRAI	FR 1980-10566		19800512		
	US 1981-261935		19810508		

AB A process is described for manufacturing a substrate-fed logic operator (SFL) which includes single collector **NPN** bipolar **vertical transistors**, or a **PNP** injection **transistor** and an **NPN** multicollector **transistor**, on a common substrate. The operator is manufactured from a low-doped P-type substrate on which are successively implanted a highly-doped P-type layer and a highly-doped N-type layer. The structure then succesively comprises an epitaxial N-layer, an average-doped P-type layer, and a highly-doped N-type layer below a metallic collector contact of the **NPN transistor** of the SFL operator. The dopants used to form successive layers are chosen based in part on their relative diffusion speeds. This structure is compatible with manufacturing on the same **Si** chip both SFL operators and classical linear bipolar transistors.

L19 ANSWER 17 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1983:497835 HCAPLUS
DN 99:97835
TI Oxide isolation process for standard RAM/PROM and lateral PNP cell RAM
IN Shideler, Jay Albert; Mishra, Umeshwar Dutt
PA Fairchild Camera and Instrument Corp., USA
SO Eur. Pat. Appl., 52 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 84465	A2	19830727	EP 1983-400012	19830104
	EP 84465	A3	19860205		
	R: DE, FR, GB, IT, NL				
	JP 58161363	A2	19830924	JP 1983-16	19830104

	US 4624046	A	19861125	US 1985-770355 19850827
	US 4961102	A	19901002	US 1988-256213 19881007
PRAI	US 1982-336802		19820104	
	US 1985-770355		19850827	
	US 1986-892979		19860804	

AB An oxide-isolated RAM (random-access memory) and PROM (programmable and read-only memory) process is disclosed wherein a RAM circuit includes a lateral **PNP transistor** formed in the same island of **Si** material as a **vertical NPN** device and further wherein contact is made to the base of the lateral PNP and to the collector of the **vertical NPN** through a buried contact region accessed through a sink region formed in an adjacent island of semiconductor material. A field implantation beneath the isolation oxide avoids implanting impurity along the sidewalls of the semiconductor material adjacent the field oxidation and therefore provides both vertical and lateral isolation from 1 **Si** island to another. Substantial redns. in sink sizes and cell sizes are obtained by eliminating the field diffusions from the sidewalls of the semiconductor islands. The lateral **PNP transistor** serves as an active load for memory circuit construction using this structure. The process also can be used to manufacture PROMs from **vertical NPN transistors** . An LVCEO (collector-emitter breakdown voltage) implant is used to increase the breakdown voltage of each **vertical transistor** from its collector-to-emitter thereby allowing junction avalanching of selected emitter base junctions to program selected PROMS in the array even though the programming voltage is only a few volts beneath the breakdown voltage of the oxide isolated structure.

IT **7440-21-3**, uses and miscellaneous
RL: DEV (Device component use); USES (Uses)
(memory devices, oxide isolation in fabrication of)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 18 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1979:144973 HCAPLUS

DN 90:144973

TI Semiconductor device

IN Tokumaru, Yukuya; Nakai, Masanori

PA Tokyo Shibaura Electric Co., Ltd., Japan

SO Brit., 5 pp.
CODEN: BRXXAA

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 1528030	A	19781011	GB 1975-53015	19751229
	JP 52017777	A2	19770209	JP 1975-93762	19750731
	DE 2558974	A1	19770203	DE 1975-2558974	19751229
	FR 2319979	A1	19770225	FR 1975-40000	19751229
	FR 2319979	B1	19780630		
PRAI	JP 1975-93762		19750731		

AB The manufacture of a high speed operable semiconductor device with small power

dissipation and no current hopping is described comprising transistors of different conductivity types formed to constitute a logic circuit, e.g. a NAND circuit. A π or P- conductivity-type **Si** substrate is formed on an N+ conductivity-type **Si** substrate, the former substrate having a lower B-impurity concentration than the latter. A SiO2 insulating film is formed on the P--type substrate in a high-temperature oxidizing atmospheric Openings in the SiO2 film are made by photoetching to permit N-type regions to be formed in the P--type substrate by thermal diffusion of P. Further similar processes result in a semiconductor device consisting of a lateral **PNP transistor**, a **vertical NPN transistor**, and 3 Schottky diodes.

L19 ANSWER 19 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1975:67303 HCAPLUS
DN 82:67303
TI Metal-**silicon** field effect transistor
IN Wilenken, Richard N.; Pearce, Leon B.
PA Intersil, Inc.
SO Ger. Offen., 15 pp.
CODEN: GWXXBX
DT Patent
LA German
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 2415736	A1	19741024	DE 1974-2415736	19740401
	CA 997869	A1	19760928	CA 1973-186913	19731128
	NL 7317176	A	19741015	NL 1973-17176	19731214
	GB 1443999	A	19760728	GB 1973-59390	19731221
	FR 2225844	A1	19741108	FR 1974-545	19740108
	JP 50003585	A2	19750114	JP 1974-10574	19740124
	IT 1008753	A	19761130	IT 1974-47931	19740125
PRAI	US 1973-350587		19730412		

AB An improved MOSFET (MOS field-effect transistor), with n- or p-type channel, operates at low threshold voltage, due to the use of a diode, formed between the **Si** substrate and the gate electrode. Two complementary units, one with p-, the other with n-type channel, can be formed on the same substrate; the design includes an n-type epitaxial layer containing a buried p-type layer, a **vertical npn transistor**, and a horizontal **pnp transistor**.

L22 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:691329 HCAPLUS
DN 131:280294
TI **Vertical** bipolar **transistor**, in particular with **SiGe** base heterojunction, and method for making same
IN Chantre, Alain
PA France Telecom, Fr.
SO PCT Int. Appl., 21 pp.
CODEN: PIXXD2
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 9954939	A1	19991028	WO 1999-FR867	19990414
	W: JP, US				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	FR 2778022	A1	19991029	FR 1998-5019	19980422
	FR 2778022	B1	20010713		
	EP 1074051	A1	20010207	EP 1999-913403	19990414
	R: DE, GB, IT, NL				
	JP 2002512452	T2	20020423	JP 2000-545198	19990414
	US 6384469	B1	20020507	US 2000-674021	20001023
PRAI	FR 1998-5019	A	19980422		
	WO 1999-FR867	W	19990414		

AB The semiconductor **region** of an **intrinsic** collector is surrounded with a lateral insulating region. A semi-conducting layer comprising a **SiGe** heterojunction is partially located between the transmitter and the intrinsic collector and extends on either side of the transmitter above the lateral insulating region. The base **intrinsic region** is formed in said semi-conducting layer with heterojunction between the transmitter and the intrinsic collector. The **base extrinsic region** and the collector **extrinsic region** resp. comprise first zones formed in said semi-conducting layer with heterojunction, located resp. on either side of the transmitter and above the lateral insulating region first part and mutually elec. insulated by the lateral insulating region second part.

IT **7440-21-3**, **Silicon**, processes **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**vertical** bipolar **transistor** with **SiGe** base heterojunction and method for making it)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4

Si 7440-21-3

RE.CNT 8 THERE ARE 8 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:659599 HCAPLUS
DN 131:265843
TI A bipolar transistor having low **extrinsic base** resistance
IN Jerome, Rick C.
PA UTMC Microelectronic Systems Inc., USA
SO PCT Int. Appl., 21 pp.
CODEN: PIXXD2
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI WO 9952138	A1	19991014	WO 1999-US7644	19990407

W: JP, KR
RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE

PRAI US 1998-56536 19980408

AB A method is disclosed for forming a **vertical** bipolar **transistor** having a relatively low value of **extrinsic base** resistance. The method creates the transistor having a recessed emitter and a single polysilicon layer that functions as the emitter contact. The polysilicon emitter contact extends downward into a shallow trench formed in an upper portion of a layer of **silicon** that is heavily doped to form the **extrinsic base regions** on each side of the shallow trench. At the bottom of the shallow trench is the single crystal emitter **region** which overlies the **intrinsic** base **region** of the transistor. In turn, the **intrinsic** base **region** overlies the collector region.

IT **7440-21-3**, **Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(**vertical** bipolar **transistor** having low **extrinsic base** resistance)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L22 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1992:603331 HCAPLUS
DN 117:203331
TI Fabrication of bipolar transistors
IN Naruse, Kazufumi
PA Sharp Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF

DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04116933	A2	19920417	JP 1990-237831	19900907
PRAI	JP 1990-237831		19900907		

AB Fabrication of a bipolar **transistor**, which contains **vertically** positioned emitter, collector, and base regions, includes (a) forming an oxide film on a substrate which is to become the emitter and base regions; (b) forming a poly-**Si** film, in which an n-type impurity is diffused, on the oxide film; (c) forming a nitride film on the poly-**Si** film, and etching it leaving only in the emitter region; (d) implanting ions in an **external base region** with the nitride film as a mask; (e) oxidizing the whole poly-**Si** film; (f) removing the nitride film and the poly-**Si**; (g) opening an area to become an emitter region; and (h) forming the emitter **region** and an **intrinsic** base **region**. The bipolar transistor is capable of fast operation.

IT **7440-21-3**, **Silicon**, reactions
RL: PRP (Properties); TEM (Technical or engineered material use); USES (Uses)
(polycryst., oxidation of, in fabrication of bipolar transistors)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L24 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1985:88633 HCAPLUS
DN 102:88633
TI Semiconductor Bi-CMOS device
IN Iwasaki, Hiroshi
PA Toshiba Corp., Japan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 4484388	A	19841127	US 1983-504161	19830614
PRAI JP 1982-108069		19820623		

AB A bipolar transistor and complementary MOS transistors may be formed on a single substrate while securing the optimal characteristics of both types of transistors. A method for forming a Bi-CMOS structure, wherein a **vertical npn transistor** and CMOS transistors are formed on a single semiconductor substrate, is disclosed. After forming a p-type epitaxial **Si** layer on a p-type **Si** substrate with a plurality of a+-type buried layers therein, n-type wells are formed to extend to the n+-type buried layers. Selective oxidation is performed to form field oxide films so as to define an n-type element region for the npn transistor, an n-type element region for the p-channel MOS transistor, and a p-type element region for the n-channel MOS transistor. An oxide film as a gate oxide film for the CMOS is formed on the surfaces of all the element regions. After forming a p-type active base region of the npn transistor by ion-implantation of B, an emitter electrode comprising an As-doped polysilicon layer is formed in contact with the p-type active base region. Gate electrodes of the CMOS are formed and have a low resistance due to doping with P and/or As. Using the emitter electrode as a diffusion source, an n-type emitter region is formed. B is then ion-implanted to simultaneously form a p+-type **external base region** and p+-type source and drain regions of the p-channel MOS transistor. P is ion-implanted to form an n+-type collector contact region and n+-type source and drain regions of the n-channel MOS transistor. A structure may be obtained which has a bipolar transistor with high **cut-off frequency** and a low power consumption and complementary MOS transistors with high switching speed characteristics.

L25 ANSWER 1 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:569005 HCAPLUS
DN 139:125984
TI Fabrication of **vertical** bipolar **transistors** showing improved high-frequency characteristics
IN Iwanaga, Junko; Matsuno, Toshinobu
PA Matsushita Electric Industrial Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 2003209116	A2	20030725	JP 2002-4208	20020111
PRAI JP 2002-4208		20020111		

AB In the process, the lateral dimension of intrinsic base layers (e.g., **Si-Ge** alloys) are reduced as follows; etching **silica** layers on intrinsic base layers through resist patterns to expose both edges of the base layers, etching the exposed base edges with liquid etchants to expose n-type epitaxial layers and form spaces for **external base** electrodes. The distance from emitter-**base** junction to **external base** electrodes is reduced as above, resulting in reduction of carrier transport time.
IT **11148-21-3**
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(intrinsic bases; manufacture of **vertical** bipolar **transistors** having reduced base resistance and showing improved high-frequency characteristics)
RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

IT **7440-21-3, Silicon**, processes
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(p-conductive, intrinsic bases; manufacture of **vertical** bipolar **transistors** having reduced base resistance and showing improved high-frequency characteristics)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 2 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:657760 HCAPLUS
DN 135:219676
TI Vertical semiconductor devices for high withstand-voltage MOSFETs

IN Uesugi, Tsutomu; Kodama, Masato
PA Toyota Central Research and Development Laboratories, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001244461	A2	20010907	JP 2000-50748	20000228
PRAI	JP 2000-50748		20000228		

AB The title devices have a super-junction vertical MOSFET where 1st and 2nd semiconductor regions are alternately and vertically provided across the elec. current direction. The insulator **regions** are provided **outside** the **Si** single **region** wherein the insulator region is provided by burying a **Si** oxide film in the trench to give the insulator region.
IT **7440-21-3P, Silicon,** properties
RL: DEV (Device component use); PNU (Preparation, unclassified); PRP (Properties); PREP (Preparation); USES (Uses)
(vertical semiconductor devices for high withstand-voltage MOSFETs)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 3 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:225356 HCAPLUS
DN 134:230757
TI Method for fabricating a self-aligned **vertical** bipolar **transistor**
IN Chantre, Alain; Marty, Michel; Baudry, Helene
PA Stmicroelectronics S. A., Fr.
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1087424	A1	20010328	EP 2000-402612	20000921
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	FR 2799048	A1	20010330	FR 1999-11895	19990923
	FR 2799048	B1	20030221		
	JP 2001244275	A2	20010907	JP 2000-283976	20000919
	JP 3386787	B2	20030317		
	US 6551891	B1	20030422	US 2000-668428	20000922
	US 2003155611	A1	20030821	US 2003-378198	20030303
PRAI	FR 1999-11895	A	19990923		
	US 2000-668428	A3	20000922		

AB The title fabrication comprises a phase of manufacturing of a **base region** comprising an **extrinsic** and intrinsic **base**, and a manufacturing of an emitter region comprising a block emitter possessing a lower part more narrow situated in an emitter window

above the intrinsic base. The manufacturing of the **extrinsic base** comprises an implantation of dopants effected after a delimiting of the emitter window, on both sides at a predetd. distance of the lateral limits of the emitter window, in a self-aligned fashion with this window emitter, in advance of the formation of the block emitter.

IT **7440-21-3, Silicon**, processes **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for fabricating self-aligned **vertical** bipolar **transistor**)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

RE.CNT 1 THERE ARE 1 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L25 ANSWER 4 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:277443 HCAPLUS
DN 129:22151
TI Semiconductor devices having **vertical** bipolar **transistors** and their manufacture
IN Takahashi, Seiichi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10116836	A2	19980506	JP 1996-268362	19961009
	JP 3022343	B2	20000321		
PRAI	JP 1996-268362		19961009		

AB The device has a refractory metal silicide layer, which is prepared by reaction of the refractory metal with **Si** under lamp annealing and removal of the residual refractory metal, on the **extrinsic base region**, which has narrow and wide portions in its region facing the longer side of the emitter diffusion layer, and a contact hole formed only on the wide portion for connection of the base electrode wiring. Base-collector capacitance is lowered by decrease of the area of the **extrinsic base region**, and increase of **extrinsic base** resistance is compensated by formation of the silicide layer.

L25 ANSWER 5 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1996:598927 HCAPLUS
DN 125:236172
TI Prismatic bipolar transistors and manufacture thereof
IN Ri, Kiko; Ri, Shinko
PA Korea Electron Transmission, Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 08186123	A2	19960716	JP 1994-316866	19941220
JP 2731811	B2	19980325		
PRAI JP 1994-316866		19941220		

AB The title process comprises formation of a 1st and a 2nd prismatic structure by formation of trenches in a 1st conductivity type **Si** substrate, implantation of a 2nd conductivity type impurity to a high concentration into a desire region of the substrate including the surrounding of the lower end of the 1st prismatic structure and the entire portion of the 2nd prismatic structure forming the collector (or emitter) region, formation of an oxide and a polycryst. **Si** film on the entire surface for an even surface, and etching thereof forming **extrinsic base regions** surrounded by the oxide film in the trenches, formation of contacts by etching of the oxide film on the side walls of the 1st prismatic structure of filling of the etched portion with polycryst. **Si**, deposition of a 2nd oxide and a polycryst. **Si** film and formation of an even surface by polishing using the 2nd oxide film as a stopper, exposure of the 1st prismatic structure by removal of the 2nd oxide film thereon, formation of the base region connected to the contact and subsequently the emitter (or collector) region by ion implantation of a 1st and a 2nd conductivity type impurity, resp., formation of a 2nd conductivity type polycryst. **Si** film wider than the emitter region on the emitter region, and formation of a protective film on the entire surface and wiring of electrodes through openings in self-alignment. Base-collector and base-emitter junction parasitic capacitance can be made min.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufacture of transistors with prismatic structures)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 6 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:178664 HCAPLUS
DN 122:69128
TI A low-capacitance bipolar/BiCMOS isolation technology, part I - concept, fabrication process, and characterization
AU Burghartz, Joachim N.; McIntosh, Robert C.; Stanis, Carol L.
CS IBM Research Division, T. J. Watson Research Center, Yorktown Heights, NY,

10598, USA
SO IEEE Transactions on Electron Devices (1994), 41(8), 1379-87
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB A device isolation structure for low-parasitic bipolar transistor integration is presented. The concept involves two selective epitaxial growth steps (SEG) and two polishing cycles which replace the collector-epitaxy and the deep/shallow trench formation in conventional device isolation. With an optimum device layout, the collector-substrate capacitance is reduced to .simeq.30%, the collector-base capacitance to .simeq.70%, and the **extrinsic base** contact resistance to <50% compared to trench isolation. The combination of SEG and polishing makes it possible to form SOI regions with locally different SOI thicknesses on the same water, so that fully depleted CMOS and **vertical** bipolar **transistors** can be combined in a SOI-BiCMOS technol.
IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(device isolation structure for low-parasitic bipolar transistor integration)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 7 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1993:438922 HCAPLUS
DN 119:38922
TI Manufacture of bipolar complementary MOS devices
IN Won, Tae Y.; Kim, Moon H.; Yoo, Kwang D.; Yoo, Ji H.
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5196356	A	19930323	US 1992-874612	19920427
JP 05218314	A2	19930827	JP 1992-251164	19920921
JP 2528242	B2	19960828		
PRAI KR 1991-20269		19911114		

AB The emitter and base of a **vertical pnp transistor** are self-aligned, an **extrinsic base** is formed by using a base electrode polysilicon layer as a diffusion source, and the base electrode and an intrinsic base are coupled by diffusion of n-type impurities, using the n+-polysilicon as a diffusion source. The process is simplified and the resistance of the **extrinsic base** is decreased.
IT **7440-21-3P, Silicon**, uses
RL: IMF (Industrial manufacture); PRP (Properties); PREP (Preparation)
(polycryst., bipolar complementary MOS devices containing, manufacture of)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 8 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1989:240873 HCAPLUS
DN 110:240873
TI An advanced single-level polysilicon submicrometer BiCMOS technology
AU Brassington, Michael P.; El-Diwany, Monir H.; Razouk, Reda R.; Thomas, Michael E.; Tuntasood, Prateep T.
CS Fairchild Res. Cent., Palo Alto, CA, 94304, USA
SO IEEE Transactions on Electron Devices (1989), 36(4, Pt. 1), 712-19
CODEN: IETDAI; ISSN: 0018-9383
DT Journal
LA English
AB An advanced very large-scale integration technol. uncompromised, high-performance n-p-n bipolar (fr = 9 GHz) and submicrometer gate-length MOS transistors is described. This technol. is intended for high-speed logic circuits operating at 5 V and where a high level of circuit integration and low power consumption is required. Features include **vertical** n-p-n **transistors** with walled, self-aligned polysilicon emitters and lightly doped **extrinsic base** extensions. MOS transistors feature complementary-doped polysilicon gates and lightly doped drain structures for both N-channel and P-channel MOS. Optional buried contacts between the polysilicon layer and all junctions in the **Si** substrate are provided. Polysilicon emitters, MOS gates, base/collector and source/drain regions are silicided. In addition, a fully planarized metal interconnect scheme incorporating nonselective chemical-vapor-deposited W and vertical-walled contacts and vias is utilized. This technol. is scalable to deep submicron (<0.5 μm) dimensions.
IT **7440-21-3**, **Silicon**, uses and miscellaneous
RL: USES (Uses)
(bipolar complementary MOS, technol. of submicrometer, for very large-scale integration applications)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L25 ANSWER 9 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1989:146207 HCAPLUS
DN 110:146207
TI Heterojunction bipolar transistor and its fabrication
PA International Business Machines Corp., USA
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 63268276	A2	19881104	JP 1988-35458	19880219
	JP 05053299	B4	19930809		

EP 288681 B1 19940824 EP 1988-102728 19880224
R: DE, FR, GB, IT
PRAI US 1987-41812 19870423
AB The transistor comprises the following: (1) a single-crystal multilayer structure having a 1st wide-gap semiconductor layer (e.g., GaAs), 2nd narrow-gap semiconductor layer (e.g., **Ge**), and 3rd wide-gap semiconductor layer (e.g., GaAs); (2) bipolar-**transistor** active regions from **vertically** arranged portions of the 1st, 2nd and 3rd layers; (3) high-resistance doped **regions** from the **outsides** of the active **regions** of the 1st and 3rd layers; and (4) a highly conductive **region** of the **outside** of the active **region** of the 1st and 3rd layers; and (4) a highly conductive **region** of the **outside** of the active **region** of the 2nd layer. The title method involves the following steps: (1) forming the single-crystal structure having the active regions; (2) forming an impurity-implantation mask for defining the device region on the 1st semiconductor layer; (3) doping the 1st, 2nd, and 3rd layers to form highly resistive and highly conductive regions; (4) forming an etching mask on the surface of the 1st layer exposed by the implantation and etching masks to expose the 2nd layer; and (5) forming ohmic contacts on the exposed 2nd layer, as well as on the 1st and 3rd layers. The emitter and base contacts of the transistor can be exchanged, and the transistor has a decreased occupying area.
IT **7440-56-4**, **Germanium**, uses and miscellaneous
RL: USES (Uses)
(transistors from gallium arsenide and, heterojunction bipolar)
RN 7440-56-4 HCAPLUS
CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

RL: TEM (Technical or engineered material use); USES (Uses)
(transistors, bipolar, heterojunction, **germanium**-gallium arsenide

L25 ANSWER 10 OF 10 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1981:543107 HCAPLUS
DN 95:143107
TI **Vertical** bipolar **transistor** structure
IN Magdo, Ingrid Emese; Rupprecht, Hans Stephen
PA International Business Machines Corp. , USA
SO Eur. Pat. Appl., 35 pp.
CODEN: EPXXDW
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 32550	A1	19810729	EP 1980-107626	19801204
EP 32550	B1	19850313		
R: DE, FR, GB, IT				
CA 1142267	A1	19830301	CA 1980-365496	19801126
US 4485552	A	19841204	US 1982-399927	19820719

PRAI US 1980-113168 19800118
AB A method for fabricating a **Si** integrated complementary **vertical** bipolar **transistor** structure consists of (1)

following a control region of low defect concentration of a 1st conductivity type in a substrate of a 2nd conductivity type, (2) forming a subcollector zone of a 2nd type in the control region, (3) forming a subcollector zone of the 1st conductivity type of a complementary transistor **outside** the control **region**, (4) forming isolation regions between the transistors, (5) depositing epitaxially a 2nd-type conductivity layer, and (6), placing base and emitter zones above the collector regions with the emitter zone formed by ion implantation and diffusion of doped polycryst. **Si** give a pnp-integrated transistor.

L31 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:71766 HCAPLUS
DN 138:129799
TI Method to form and/or isolate **vertical transistors**
IN Quek, Elgin; Sundaresan, Ravi; Pan, Yang; Lee, Yong Meng; Leung, Ying Keung; Pradeep, Yelehanka Ramachandramurthy; Zheng, Jia Zhen; Chan, Lap
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6511884	B1	20030128	US 2001-972503	20011009
PRAI	US 2001-972503		20011009		

AB The present invention relates generally to fabrication of semiconductor devices, and more specifically to methods of fabricating **vertical transistors**. The method of fabricating an isolated **vertical transistor** comprises the following steps. A wafer having a 1st implanted region selected from the group comprising a source region and a drain region is provided. The wafer further includes shallow trench isolation (STI) areas on either side of a center transistor area. The wafer is patterned down to the 1st implanted region to form a vertical pillar within the center transistor area using a patterned hard **mask**. The vertical pillar having side walls. A pad dielec. layer is formed over the wafer, lining the vertical pillar. A nitride layer is formed over the pad dielec. layer. The structure is patterned and etched through the nitride layer and the pad dielec. layer; and into the wafer within the STI areas to form STI trenches within the wafer. The STI trenches are filled with insulative material to form STIs within STI trenches. The patterned nitride and pad dielec. layers are removed. The patterned hard **mask** is removed. Gate oxide is grown over the exposed portions of the wafer and the vertical pillar. Spacer gates are formed over the gate oxide lined side walls of the vertical pillar. Spacer gate implants are formed within the spacer gates, and a 2nd implanted **region** is formed **within** the vertical pillar selected from the group consisting of a drain region and a source region that is not the same as the 1st implanted region to complete formation of the isolated **vertical transistor**.
IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; in isolated **vertical transistors**)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:344844 HCAPLUS
DN 127:43391
TI Vertical power MOSFET and its manufacture

IN Tsoi, Hak-yam; Tam, Pak; De, Fresart Edouard D.
PA Motorola, Inc., USA
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5631484	A	19970520	US 1995-576983	19951226
EP 782181	A2	19970702	EP 1996-119955	19961212
EP 782181	A3	19991013		
R: DE, FR, GB, IT				
JP 09186173	A2	19970715	JP 1996-354014	19961218
PRAI US 1995-576983		19951226		

AB A method for forming a semiconductor device includes forming insulated gate regions on a substrate using a 1st photomasking step, forming a base region through an opening between the insulated gate regions, and forming a source **region within** the **base region**. Next, a protective layer is formed and selectively patterned using a 2nd photomasking step to form an opening within the 1st opening and an opening above one of the insulated gate regions. Next, a portion of the substrate and a portion of the insulated gate region are removed. Ohmic contacts are then formed and patterned using a 3rd photomasking step. Addnl., a termination structure is described.

L31 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1996:537780 HCAPLUS
DN 125:210433
TI Simultaneous fabrication of a **vertical** bipolar **transistor** and a memory cell
IN Sung, Janmye
PA Vanguard International Semiconductor Corp., Taiwan
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 5547893	A	19960820	US 1995-578923	19951227
PRAI US 1995-578923		19951227		

AB The present invention provides a method of simultaneously forming CMOS DRAM cells, CMOS devices, and **vertical** bipolar **transistors** on the same chip. The invention utilizes a CMOS DRAM process to simultaneously fabricate a **vertical** bipolar **transistor** and uses only 1 addnl. **mask** (a base implant **mask**) compared to forming the DRAM cell alone. Also, to reduce the bipolar collector plug resistance, the process uses a W-plug module where the collector is formed **within** a field oxide **region** near the base.
IT **7440-21-3**, **Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; simultaneous fabrication of **vertical** bipolar **transistors** and memory cells containing)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L31 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:797295 HCAPLUS
DN 123:185374
TI Semiconductor devices and manufacture thereof
IN Sato, Fumihiko
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07106341	A2	19950421	JP 1993-251254	19931007
	JP 2551353	B2	19961106		
	US 5432104	A	19950711	US 1994-319638	19941007
PRAI	JP 1993-251254		19931007		

AB The title process comprises sequential formation of a 2nd conductivity type buried layer selectively on a 1st conductivity type single crystal **Si** substrate, a 2nd conductivity type **Si** epitaxial layer on the entire surface, a device isolation field oxide film, a 1st insulating film of a desired thickness on the entire surface, a 1st conductivity type 1st polycryst. semiconductor film in a desired shape, and a 2nd insulating film on the entire surface; sequential etching of a desired region of the 2nd insulating film and at least the 1st polycryst. semiconductor film forming a 1st opening reaching the 1st insulating film; deposition of a 3rd insulating film on the entire surface and anisotropic etching thereof forming a 1st insulating spacer in the 1st opening; isotropic etching of the 1st insulating film with a **mask** from the 2nd insulating film and the 1st insulating spacer to form a 2nd opening reaching the **Si** epitaxial layer and having an opening area wider than that of the 1st opening and protrusion of the 1st polycryst. semiconductor layer; simultaneous formation of a 1st conductivity type 2nd polycryst. semiconductor film of a desired thickness on the bottom of the 1st polycryst. semiconductor film protruded with a 1st conductivity type 1st single crystal semiconductor layer on the **Si** epitaxial layer exposed in the 2nd opening by selective growth of the 1st semiconductor film; simultaneous formation of a 1st conductivity type 3rd polycryst. semiconductor film of a desired thickness on the bottom of the 2nd polycryst. Semiconductor film with a 1st conductivity type 2nd single crystal semiconductor layer higher in impurity concentration than that in the 1st single crystal semiconductor layer and in contact with the bottom of the 3rd polycryst. semiconductor film on the 1st single crystal semiconductor layer by selective growth of the 2nd semiconductor film; implantation of a 2nd conductivity type ions using a **mask** from the 2nd insulating film and the 1st insulating spacer to convert the 1st single crystal semiconductor layer immediate below the gap of the 1st insulating spacer to a 3rd single crystal semiconductor layer higher in impurity concentration than in the **Si** epitaxial layer; deposition of a 4th insulating film on the entire surface and anisotropic etching thereof forming a 2nd insulating spacer on the side of the 1st insulating spacer; formation of a 2nd conductivity type 4th single crystal semiconductor layer filling the gap of the 2nd insulating spacer and

covering the 2nd single crystal semiconductor layer by selective growth of the 3rd semiconductor layer. Especially a **vertical** bipolar **transistor** is prepared, and parasite capacitance between the base and the collector region can be lowered and connection of an **intrinsic base region** from the 2nd single crystal semiconductor layer to a base draw-out electrode from the 1st polycryst. semiconductor film is made without any obstacle.

IT **7440-21-3, Silicon,** uses
RL: DEV (Device component use); USES (Uses)
(epitaxial formation of **intrinsic base regions** in openings of semiconductor devices)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(film; for epitaxy of **intrinsic base regions** in **vertical** bipolar **transistors**)
RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L31 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1984:28696 HCAPLUS
DN 100:28696
TI Fabrication method for **vertical pnp** structure with Schottky barrier diode emitter utilizing ion implantation
IN De Bar, David E.; Hamaker, Raymond W.; Stephens, Geoffrey B.
PA International Business Machines Corp. , USA
SO U.S., 10 pp. Cont. of U.S. Ser. No. 142,323 ab
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4412376	A	19831101	US 1982-355059	19820305
PRAI	US 1979-25693		19790320		
	US 1980-142323		19800421		

AB A **vertical pnp** bipolar **transistor** with Schottky-barrier diode emitter has simplified structure and process steps for combining a complementary pnp in an npn **Si** integrated circuit. The speed and d. of the vertical p-n-p are improved. The structure uses a sep. **masked** ion/implant for the npn **intrinsic base** implant (which also forms the pnp collector region) so that the pnp base doping profile can intercept the pnp collector profile at a lower concentration resulting in lower collector/base

capacitance, lower series collector resistance, and higher collector/base breakdown voltage. In particular, the n-type conductivity base regions are formed by ion-implanting P at 200 keV and a dose of .apprx.2 + 1012 cm -2. Schottky-barrier contacts are formed by vacuum evaporating an Al-**Si** alloy (e.g. containing 1.5% **Si**), followed by annealing at .apprx.450° for 1 h.

L31 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1982:153961 HCAPLUS
DN 96:153961
TI Fabricating semiconductor devices
IN Shinbo, Masafumi
PA Daini Seikosha Co., Ltd., Japan
SO Brit. UK Pat. Appl., 13 pp.
CODEN: BAXXDU
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 2072945	A	19811007	GB 1981-6841	19810304
	GB 2072945	B2	19840125		
	US 4380481	A	19830419	US 1981-244793	19810317
PRAI	JP 1980-39463		19800327		

AB An improved method is described of manufacturing **vertical**-type static induction **transistors** or FETs having a gate region encircling a source or drain region. A multiinsulation island layer composed of antioxidn. and oxide films, e.g. Si3N4 and SiO2, is formed on the surface of an n- epitaxial layer. A selective oxidation layer is formed on the n-epitaxial layer using the nitride film as a **mask**. A 1st window is defined having a width determined by the side faces of the multiinsulation layer, after a 1st side etching step, and an end of the selective oxidation film. A p+ gate region is formed by selective diffusion of an impurity. The size of the nitride film is reduced by subjecting the multiinsulation layer to a 2nd side etching step and carrying out selective oxidation An n+ drain **region** is formed **within** the p+ **region** after removing the multiinsulation layer thereby defining a 2nd window.

L31 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:71766 HCAPLUS
DN 138:129799
TI Method to form and/or isolate **vertical transistors**
IN Quek, Elgin; Sundaresan, Ravi; Pan, Yang; Lee, Yong Meng; Leung, Ying Keung; Pradeep, Yelehanka Ramachandramurthy; Zheng, Jia Zhen; Chan, Lap
PA Chartered Semiconductor Manufacturing Ltd., Singapore
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 6511884	B1	20030128	US 2001-972503	20011009
PRAI US 2001-972503		20011009		

AB The present invention relates generally to fabrication of semiconductor devices, and more specifically to methods of fabricating **vertical transistors**. The method of fabricating an isolated **vertical transistor** comprises the following steps. A wafer having a 1st implanted region selected from the group comprising a source region and a drain region is provided. The wafer further includes shallow trench isolation (STI) areas on either side of a center transistor area. The wafer is patterned down to the 1st implanted region to form a vertical pillar within the center transistor area using a patterned hard **mask**. The vertical pillar having side walls. A pad dielec. layer is formed over the wafer, lining the vertical pillar. A nitride layer is formed over the pad dielec. layer. The structure is patterned and etched through the nitride layer and the pad dielec. layer; and into the wafer within the STI areas to form STI trenches within the wafer. The STI trenches are filled with insulative material to form STIs within STI trenches. The patterned nitride and pad dielec. layers are removed. The patterned hard **mask** is removed. Gate oxide is grown over the exposed portions of the wafer and the vertical pillar. Spacer gates are formed over the gate oxide lined side walls of the vertical pillar. Spacer gate implants are formed within the spacer gates, and a 2nd implanted **region** is formed **within** the vertical pillar selected from the group consisting of a drain region and a source region that is not the same as the 1st implanted region to complete formation of the isolated **vertical transistor**.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; in isolated **vertical transistors**)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L31 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1997:344844 HCAPLUS
DN 127:43391
TI Vertical power MOSFET and its manufacture

IN Tsoi, Hak-yam; Tam, Pak; De, Fresart Edouard D.
PA Motorola, Inc., USA
SO U.S., 21 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5631484	A	19970520	US 1995-576983	19951226
	EP 782181	A2	19970702	EP 1996-119955	19961212
	EP 782181	A3	19991013		
	R: DE, FR, GB, IT				
	JP 09186173	A2	19970715	JP 1996-354014	19961218
PRAI	US 1995-576983		19951226		

AB A method for forming a semiconductor device includes forming insulated gate regions on a substrate using a 1st photomasking step, forming a base region through an opening between the insulated gate regions, and forming a source **region within** the **base region**. Next, a protective layer is formed and selectively patterned using a 2nd photomasking step to form an opening within the 1st opening and an opening above one of the insulated gate regions. Next, a portion of the substrate and a portion of the insulated gate region are removed. Ohmic contacts are then formed and patterned using a 3rd photomasking step. Addnl., a termination structure is described.

L31 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1996:537780 HCAPLUS
DN 125:210433
TI Simultaneous fabrication of a **vertical** bipolar **transistor** and a memory cell
IN Sung, Janmye
PA Vanguard International Semiconductor Corp., Taiwan
SO U.S., 19 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5547893	A	19960820	US 1995-578923	19951227
PRAI	US 1995-578923		19951227		

AB The present invention provides a method of simultaneously forming CMOS DRAM cells, CMOS devices, and **vertical** bipolar **transistors** on the same chip. The invention utilizes a CMOS DRAM process to simultaneously fabricate a **vertical** bipolar **transistor** and uses only 1 addnl. **mask** (a base implant **mask**) compared to forming the DRAM cell alone. Also, to reduce the bipolar collector plug resistance, the process uses a W-plug module where the collector is formed **within** a field oxide **region** near the base.
IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; simultaneous fabrication of **vertical** bipolar **transistors** and memory cells containing)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L31 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:797295 HCAPLUS
DN 123:185374
TI Semiconductor devices and manufacture thereof
IN Sato, Fumihiko
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07106341	A2	19950421	JP 1993-251254	19931007
	JP 2551353	B2	19961106		
	US 5432104	A	19950711	US 1994-319638	19941007
PRAI	JP 1993-251254		19931007		

AB The title process comprises sequential formation of a 2nd conductivity type buried layer selectively on a 1st conductivity type single crystal **Si** substrate, a 2nd conductivity type **Si** epitaxial layer on the entire surface, a device isolation field oxide film, a 1st insulating film of a desired thickness on the entire surface, a 1st conductivity type 1st polycryst. semiconductor film in a desired shape, and a 2nd insulating film on the entire surface; sequential etching of a desired region of the 2nd insulating film and at least the 1st polycryst. semiconductor film forming a 1st opening reaching the 1st insulating film; deposition of a 3rd insulating film on the entire surface and anisotropic etching thereof forming a 1st insulating spacer in the 1st opening; isotropic etching of the 1st insulating film with a **mask** from the 2nd insulating film and the 1st insulating spacer to form a 2nd opening reaching the **Si** epitaxial layer and having an opening area wider than that of the 1st opening and protrusion of the 1st polycryst. semiconductor layer; simultaneous formation of a 1st conductivity type 2nd polycryst. semiconductor film of a desired thickness on the bottom of the 1st polycryst. semiconductor film protruded with a 1st conductivity type 1st single crystal semiconductor layer on the **Si** epitaxial layer exposed in the 2nd opening by selective growth of the 1st semiconductor film; simultaneous formation of a 1st conductivity type 3rd polycryst. semiconductor film of a desired thickness on the bottom of the 2nd polycryst. Semiconductor film with a 1st conductivity type 2nd single crystal semiconductor layer higher in impurity concentration than that in the 1st single crystal semiconductor layer and in contact with the bottom of the 3rd polycryst. semiconductor film on the 1st single crystal semiconductor layer by selective growth of the 2nd semiconductor film; implantation of a 2nd conductivity type ions using a **mask** from the 2nd insulating film and the 1st insulating spacer to convert the 1st single crystal semiconductor layer immediate below the gap of the 1st insulating spacer to a 3rd single crystal semiconductor layer higher in impurity concentration than in the **Si** epitaxial layer; deposition of a 4th insulating film on the entire surface and anisotropic etching thereof forming a 2nd insulating spacer on the side of the 1st insulating spacer; formation of a 2nd conductivity type 4th single crystal semiconductor layer filling the gap of the 2nd insulating spacer and

covering the 2nd single crystal semiconductor layer by selective growth of the 3rd semiconductor layer. Especially a **vertical** bipolar **transistor** is prepared, and parasite capacitance between the base and the collector region can be lowered and connection of an **intrinsic base region** from the 2nd single crystal semiconductor layer to a base draw-out electrode from the 1st polycryst. semiconductor film is made without any obstacle.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(epitaxial formation of **intrinsic base regions** in openings of semiconductor devices)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(film; for epitaxy of **intrinsic base regions** in **vertical** bipolar **transistors**)
RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L31 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1984:28696 HCAPLUS
DN 100:28696
TI Fabrication method for **vertical pnp** structure with Schottky barrier diode emitter utilizing ion implantation
IN De Bar, David E.; Hamaker, Raymond W.; Stephens, Geoffrey B.
PA International Business Machines Corp. , USA
SO U.S., 10 pp. Cont. of U.S. Ser. No. 142,323 ab
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 4412376	A	19831101	US 1982-355059	19820305
PRAI	US 1979-25693		19790320		
	US 1980-142323		19800421		

AB A **vertical pnp** bipolar **transistor** with Schottky-barrier diode emitter has simplified structure and process steps for combining a complementary pnp in an npn **Si** integrated circuit. The speed and d. of the vertical p-n-p are improved. The structure uses a sep. **masked** ion/implant for the npn **intrinsic base** implant (which also forms the pnp collector region) so that the pnp base doping profile can intercept the pnp collector profile at a lower concentration resulting in lower collector/base

capacitance, lower series collector resistance, and higher collector/base breakdown voltage. In particular, the n-type conductivity base regions are formed by ion-implanting P at 200 keV and a dose of .apprx.2 + 1012 cm -2. Schottky-barrier contacts are formed by vacuum evaporating an Al-**Si** alloy (e.g. containing 1.5% **Si**), followed by annealing at .apprx.450° for 1 h.

L31 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1982:153961 HCAPLUS
DN 96:153961
TI Fabricating semiconductor devices
IN Shinbo, Masafumi
PA Daini Seikosha Co., Ltd., Japan
SO Brit. UK Pat. Appl., 13 pp.
CODEN: BAXXDU
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	GB 2072945	A	19811007	GB 1981-6841	19810304
	GB 2072945	B2	19840125		
	US 4380481	A	19830419	US 1981-244793	19810317
PRAI	JP 1980-39463		19800327		

AB An improved method is described of manufacturing **vertical**-type static induction **transistors** or FETs having a gate region encircling a source or drain region. A multiinsulation island layer composed of antioxidn. and oxide films, e.g. Si3N4 and SiO2, is formed on the surface of an n- epitaxial layer. A selective oxidation layer is formed on the n-epitaxial layer using the nitride film as a **mask**. A 1st window is defined having a width determined by the side faces of the multiinsulation layer, after a 1st side etching step, and an end of the selective oxidation film. A p+ gate region is formed by selective diffusion of an impurity. The size of the nitride film is reduced by subjecting the multiinsulation layer to a 2nd side etching step and carrying out selective oxidation An n+ drain **region** is formed **within** the p+ **region** after removing the multiinsulation layer thereby defining a 2nd window.

=> D L33 BIB AB TOT HITSTR

L33 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:779912 HCAPLUS
DN 130:46224
TI Manufacture of a **germanium**-implanted heterojunction bipolar transistor
IN Lombardo, Salvatore; Pinto, Angelo; Nicotra, Maria Concetta
PA Stmicroelectronics S.r.l., Italy; CO.RI.M.ME. Consorzio Per La Ricerca Sulla Microelletronica Nel Mezzogiorno
SO Eur. Pat. Appl., 25 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 881669	A1	19981202	EP 1997-830259	19970530

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT,

IE, SI, LT, LV, FI, RO

	JP 11087364	A2	19990330	JP 1998-151595	19980601
	US 6624017	B1	20030923	US 2000-724563	20001127
	US 2004004270	A1	20040108	US 2003-615084	20030707
PRAI	EP 1997-830259	A	19970530		
	US 1998-87398	A1	19980529		
	US 2000-724563	A3	20001127		

AB A process for fabricating a **vertical** high-carrier-mobility **transistor** on a substrate of crystalline **Si** doped with **n-type** impurities, having a collector region in the lower portion of the substrate, comprises: defining a window in the semiconductor substrate; providing a 1st implantation of **Ge** atoms through the window; providing a 2nd implantation of acceptor dopants through the window to define a base region; applying an RTA treatment, or treatment in an oven, to reconstruct the crystal lattice within the substrate comprising a **Si/Ge** alloy (Si1-xGex); forming a 1st thin dielec. layer of SiO2 by CVD; depositing a 2nd dielec. layer on the 1st dielec. layer; depositing a polysilicon layer on the 2nd dielec. layer; etching away, **within** the window **region**, the 1st and 2nd dielec. layers and the polysilicon layer, to expose the base region and form isolation spacers at the window edges; and forming an **n-type emitter** in the base and window regions. This process allows the frequency field of application of HBT transistors to be extended, while eliminating deviations of the base currents from the ideal.

IT **7440-56-4, Germanium**, uses
RL: MOA (Modifier or additive use); USES (Uses)
(manufacture of a **germanium**-implanted heterojunction bipolar transistor)

RN 7440-56-4 HCAPLUS

CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(manufacture of a **germanium**-implanted heterojunction bipolar transistor containing)

RN 11148-21-3 HCAPLUS

CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; manufacture of a **germanium**-implanted heterojunction bipolar transistor containing)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L33 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:764153 HCAPLUS
DN 130:19662
TI **Vertical** bipolar semiconductor power **transistor** with an interdigitized geometry, with optimization of the base-to-emitter potential difference
IN Patti, Davide
PA Stmicroelectronics S.R.L., Italy
SO Eur. Pat. Appl., 10 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 878848	A1	19981118	EP 1997-830228	19970516
	R: DE, FR, GB, IT				
	US 6069399	A	20000530	US 1998-79827	19980515
	US 6297118	B1	20011002	US 2000-548784	20000413
PRAI	EP 1997-830228	A	19970516		
	US 1998-79827	A3	19980515		

AB The transistor comprises: an epitaxial layer with a first conductivity type; a base buried region with a second conductivity type; a sinker base region with the second conductivity type, which extends from the main surface to the buried base region, and delimits, together with the base buried region, emitter fingers in the epitaxial layer; an emitter buried region with the first conductivity type and a doping level which is higher than that of the epitaxial layer, said emitter buried region being embedded in the epitaxial layer in a position adjacent to the base buried region; and a sinker emitter region having the first conductivity type and a doping level which is higher than that of the epitaxial layer and extending from the main surface to the emitter buried **region inside** the emitter fingers. The buried and sinker emitter regions delimit in each finger pairs of sections which are mutually spaced and delimit between one another a central region of the epitaxial layer. The sinker emitter region sections of a finger extend in the vicinity of mutually facing edges of the emitter buried region sections.
IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(**vertical** bipolar semiconductor power **transistor** with an interdigitized geometry, with optimization of the base-to-**emitter p**.d.)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L36 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:551637 HCAPLUS
DN 137:102519
TI **Vertical** heterojunction bipolar **transistor**
IN El-Sharawy, El-Badawy Amien; Hashemi, Majid M.
PA National Scientific Corporation, USA
SO U.S., 16 pp., Cont.-in-part of U.S. 6,171,920.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6423990	B1	20020723	US 1999-441576	19991117
	US 5912481	A	19990615	US 1997-939487	19970929
	US 6171920	B1	20010109	US 1999-267252	19990312
	WO 2001037349	A1	20010525	WO 2000-US42206	20001116
	W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				
	US 2002179933	A1	20021205	US 2002-197726	20020717
PRAI	US 1997-939487	A3	19970929		
	US 1999-267252	A2	19990312		
	US 1999-441576	A1	19991117		

AB A heterojunction bipolar transistor is provided with a **Si** base region that forms a semiconductor junction with a multilayer **emitter** having a thin Ga arsenide **emitter** layer proximate the base region and a distal Ga phosphide **emitter** layer. The GaAs **emitter** layer is sufficiently thin, preferably <200 Å, so as to be coherently strained. In 1 embodiment, the GaP **emitter** layer includes a doped region which serves as the **emitter** and a non-doped **region** on which the **intrinsic** portion of the transistor is formed.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(**vertical** heterojunction bipolar **transistor** with wide bandgap with low interdiffusion base-**emitter** junction and fabrication)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 39 THERE ARE 39 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L36 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:809061 HCAPLUS

DN 135:337918
TI Process for formation of **vertically** isolated bipolar **transistor** device with reduced surface area
IN Kitch, Vassili
PA National Semiconductor Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6313000	B1	20011106	US 1999-442810	19991118
PRAI US 1999-442810		19991118		

AB A **vertically**-isolated bipolar **transistor** occupying reduced surface area is fabricated by circumscribing an expected active device **region within** a 1st narrow trench. The 1st trench is filled with sacrificial material impermeable to diffusion of conductivity-altering dopant, and then isolation dopant of a conductivity type opposite to that of the substrate is introduced into the trench-circumscribed **Si** region. The introduced isolation dopant is then thermally driven into the substrate, with lateral diffusion of isolation dopant phys. constrained by the existing 1st narrow trench. Epitaxial **Si** is then formed over the substrate, with polysilicon formed in regions overlying the filled narrow trench. A 2nd, wider trench encompassing the 1st trench is etched to consume epitaxial **Si**, polysilicon, and the sacrificial material. The 2nd trench is then filled with dielec. material. Base and **emitter** structures are formed in the conventional manner within the trench-circumscribed **Si**. Constraint of lateral diffusion of isolation-type dopant by the 1st trench reduces lateral dimensions of the isolation region and of the overall device. The smaller device area permits enhanced device packing d. and reduces parasitic capacitance arising between the isolation region and the substrate.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in process for formation of **vertically** isolated bipolar **transistor** device with reduced surface area)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 19 THERE ARE 19 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L36 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:493241 HCAPLUS
DN 133:113632
TI **Vertical** bipolar **transistor** with minimum variation of properties and method of manufacturing the same
IN Sato, Fumihiko
PA NEC Corporation, Japan
SO Eur. Pat. Appl., 39 pp.

CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1020923	A2	20000719	EP 2000-100084	20000105
	EP 1020923	A3	20020116		
	R: DE, FR, GB, IT, NL, SI, LT, LV, RO				
	JP 2000269233	A2	20000929	JP 1999-107420	19990415
	JP 3303833	B2	20020722		
	US 6680522	B1	20040120	US 1999-474504	19991229
	KR 2000057734	A	20000925	KR 2000-861	20000110
PRAI	JP 1999-4685	A	19990111		

AB An object of the invention is to minimize variation in characteristics of a **vertical** bipolar **transistor**. An insulating side wall spacer composed of a **Si** nitride film 10 and a **Si** oxide film 9 is formed on the side surface of an opening 101 formed in a base electrode polysilicon film 7. The thickness (= WD) of the insulating side wall spacer is made thicker than the maximum thickness (= WF) within a range of variation in thickness of a polycryst. film 12 grown from the side surface of the base electrode polysilicon film 7 exposed inside the opening 101 (namely, WD > WF). The size of an opening for forming an **emitter** electrode polysilicon film 16 on an **intrinsic base** 11 is not influenced by the thickness of a polycryst. film 12 epitaxially growing from the side surface of the polysilicon film 7 for the base electrode, but is defined by the side wall spacer formed on a portion of the side surface of the base electrode polysilicon film. Therefore, **emitter** area hardly disperses, and elec. characteristics become stable.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(poly; **vertical** bipolar **transistor** with min. variation of properties and method of manufacturing using)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

IT **12727-59-2**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(**vertical** bipolar **transistor** with min. variation of properties and method of manufacturing using)
RN 12727-59-2 HCAPLUS
CN Germanium alloy, base, Ge 0-100,Si 0-100 (9CI) (CA INDEX NAME)

Component	Component Percent	Component Registry Number
Ge	0 - 100	7440-56-4
Si	0 - 100	7440-21-3

L36 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1999:783850 HCAPLUS
DN 132:8251
TI Low noise **vertical** bipolar **transistor** and method of manufacturing it
IN Ghantre, Alain; Marty, Michel; Dutartre, Didier; Monroy, Augustin; Laurens, Michel; Guette, Francois
PA Stmicroelectronics S.A., Fr.; Commissariat A L'Energie Atomique; France Telecom
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 962966	A1	19991208	EP 1999-401337	19990603
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
FR 2779572	A1	19991210	FR 1998-7059	19980605
FR 2779572	B1	20031017		
US 6177717	B1	20010123	US 1999-323418	19990601
JP 2000031155	A2	20000128	JP 1999-156049	19990603
PRAI FR 1998-7059	A	19980605		

AB The intrinsic collector is epitaxied on a layer of the extrinsic collector buried in a semiconductor substrate. A lateral isolation region surrounds the upper part of the intrinsic collector and one realizes a well of removed extrinsic collector. One realizes a base of a **SiGe** heterojunction situated above the intrinsic collector and the lateral isolation region from nonselective epitaxy, and one realizes an in-situ-doped **emitter** by epitaxy on a predetd. window and the surface of the **base** situated above the **intrinsic** collector in a fashion to obtain ≥1 of said windows of an **emitter** region formed of single-crystal **Si** and directly in contact with **Si** of the base.
IT **7440-21-3**, **Silicon**, processes **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(low noise **vertical** bipolar **transistor** and method of manufacturing it)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L36 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1995:913513 HCAPLUS
DN 123:304415
TI Semiconductor devices
IN Sato, Fumihiko
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 14 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07201877	A2	19950804	JP 1993-336646	19931228
	JP 2626535	B2	19970702		
	US 5500554	A	19960319	US 1994-364964	19941228
PRAI	JP 1993-336646		19931228		

AB The device has a 1st conductivity type **Si** single crystal substrate having a 2nd conductivity type buried ladyer partly covered by a 2nd conductivity type **Si** epitaxial layer, a 1st SiO2 film with a 1st opening reaching the **Si** epitaxial layer, a Si3N4 film having a 2nd opening in the 1st opening on the SiO2 film, a 2nd SiO2 film having a 3rd opening in the 2nd opening on the Si3N4 film, a base draw-out electrode which has a 1st polycryst. semiconductor lower layer, a 4th opening in the 3rd opening, protrusion from the edge of the 3rd opening as formed on the 2nd SiO2 film, a 4th SiO2 film covering the base draw-out electrode, a 1st spacer from a 5th SiO2 film covering the sides of the base draw-out electrode and the 4th SiO2 film in the 4th opening, a 1st conductivity type 2nd polycryst. semiconductor film in the 2nd opening covering the top of the 1st SiO2 film, the bottom of the 2nd SiO2 film, and the side wall of the Si3N4 film in the 2nd opening, a 1st conductivity type 3rd polycryst. semiconductor film connected to the bottom of the 1st polycryst. semiconductor film and the 2nd polycryst. semiconductor film exposed in the 3rd opening, and covering the 2nd SiO2 film side wall in the 3rd opening, a 1st conductivity type 1st single crystal semiconductor layer connected to the upper surface of the **Si** epitaxial layer, and the 3rd and the 2nd polycryst. Semiconductor layer, and partly filling the 1st opening, a 2nd spacer from a 5th SiO2 film covering a part of the sides and the bottom of the 1st spacer, and sides of the 3rd polycryst. semiconductor film exposed in the 2nd and the 3rd polycryst. semiconductor film exposed in the 2nd and the 3rd opening, and the 1st single crystal semiconductor layer exposed in the 2nd opening, and a 2nd conductivity type 2nd single crystal semiconductor film covering a portion of the side of the 2nd spacer and the upper surface of the 1st single crystal semiconductor layer not covered by the 2nd spacer. The thickness of the insulating laminate between the 2nd conductivity type **Si** epitaxial collector region and the base draw-out electrode can be increased and the 1st conductivity type 1st single crystal **intrinsic base** layer under the **emitter** region in the opening can be made thin, and parasite capacitance between the collector and the base region is lowered while cutoff frequency is enhanced, especially in a **vertical** bipolar **transistor**.

IT **7440-21-3**, **Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(epitaxial base region under **emitter** regions in opening structures with insulating laminate walls)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L36 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:593473 HCAPLUS
DN 121:193473
TI **Vertical** bipolar **transistors** and their manufacture
PA Korea Institute of Electronic Communication, S. Korea
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06069219	A2	19940311	JP 1993-137514	19930608
	JP 2524079	B2	19960814		
	KR 9507348	B1	19950710	KR 1992-9982	19920609
PRAI	KR 1992-9982	A	19920609		

AB In the manufacture the n+-buried layer for the **emitter** and the **Si** layer for the **intrinsic base** formed on the -buried layer are formed on a **Si** semiconductor substrate; a trench insulating oxide film is formed for elec. isolation between elements; and a base electrode is formed for flattening and micropatterning a p+-polycryst. **Si** and silicide film. The operating voltage and switching speed of an integrated injection logic can be improved and for an **emitter** coupled logic the integration can be increased greatly.

L37 ANSWER 1 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:492318 HCAPLUS
DN 139:45254
TI Semiconductor device with a **vertical transistor** and method for fabricating the same
IN Park, Cheol Soo
PA S. Korea
SO U.S. Pat. Appl. Publ., 6 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2003116800	A1	20030626	US 2002-325392	20021219
PRAI KR 2001-84007	A	20011224		

AB The present invention relates to a semiconductor device and a method for fabricating the same, which has a **transistor** of a **vertical** structure. The fabricating method comprises: forming an insulating film on a **Si** substrate; forming a 1st conductive well of a 1st conductive type in the **Si** substrate; 1st and 2nd conductive layers of a 2nd conductive type at a portion below the surface of the 1st conductive well and in the **inner region** of the 1st conductive well, resp.; patterning the insulating film and the 1st conductive layer of the 2nd conductive type, so that contact holes are formed in such a manner that the 2nd conductive layer formed in the **inner region** of the 1st conductive well is exposed through the contact holes; forming a gate insulating film on the sidewall of the 1st conductive well in the contact holes; and forming a gate electrode on the surface of the gate insulating film in the contact holes.
IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(semiconductor device with a **vertical transistor** and method for fabricating the same)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 2 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:830454 HCAPLUS
DN 137:303328
TI Method for fabricating an insulated-gate **vertical transistor** having a quadruple conduction channel, and integrated circuit comprising this transistor
IN Skotnicki, Thomas; Josse, Emmanuel
PA STMicroelectronics SA, Fr.
SO Fr. Demande, 26 pp.
CODEN: FRXXBL
DT Patent
LA French
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI FR 2823010 A1 20021004 FR 2001-4437 20010402
FR 2823010 B1 20030815
US 2002163027 A1 20021107 US 2002-114672 20020402
PRAI FR 2001-4437 A 20010402

AB The **vertical transistor** comprises an insulated gate on a semiconductor substrate, a vertical post incorporating at its summit one of source of source and drain regions, a dielec. layer of the gate situated on the flanks of the post and on the upper surface of the substrate, and a semiconductive gate supported on a dielec. layer of the gate; the other source and drain regions extend from the lower part of the post; the insulated gate comprises an external insulated part supported on the flanks of the post, and an internal insulated part situated at the interior of the post between the source and drain **regions**; the **internal** insulated part is separated laterally from the external insulated part by 2 semiconductive connective regions extending between the source and drain regions and forming 2 very fine posts.

IT **7440-21-3, Silicon**, processes **11148-21-3**
RL: CPS (Chemical process); DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for fabricating insulated-gate **vertical transistor** having quadruple conduction channel and integrated circuit comprising this transistor)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L37 ANSWER 3 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:552255 HCAPLUS
DN 137:117938
TI Structure and method of fabricating a MOS transistor having increased substrate resistance
IN Salling, Craig T.; Wu, Zhiqiang; Hu, Che-Jen
PA Texas Instruments Incorporated, USA
SO Eur. Pat. Appl., 16 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 1225636	A2	20020724	EP 2002-100045	20020121
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR				
US 2002096716	A1	20020725	US 2002-43507	20020114
JP 2002280552	A2	20020927	JP 2002-14180	20020123

US 2003207543 A1 20031106 US 2003-446760 20030528
PRAI US 2001-263619P P 20010123
US 2002-43507 A3 20020114
AB The present invention is related in general to the field of electronic systems and semiconductor devices, and more specifically to structure and fabrication methods of MOS transistors, which have an increased substrate resistance compared to standard technol. A structure and a fabrication method are presented for a lateral MOS transistor, positioned on the surface of an integrated circuit fabricated in a semiconductor of a 1st conductivity type, comprising a source and a drain, each having at the surface a region of the opposite conductivity type extending to the centrally located gate, defining the active area of the transistor; and a semiconductor **region within** the semiconductor of the 1st conductivity type, having a resistivity higher than the remainder of the semiconductor, this region extending **vertically** below the **transistor** while laterally limited to the area of the transistor such that the resistivity under the gate is different from the resistivity under the source and drain regions.
IT **7440-21-3, Silicon**, uses **11148-21-3**
RL: DEV (Device component use); USES (Uses)
(structure and method of fabricating a MOS transistor having increased substrate resistance)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L37 ANSWER 4 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:897802 HCAPLUS
DN 134:186532
TI Vertical MOS-gated pin-diodes: MOS-gated tunneling transistors in **Si**(100) and **Si**(111)
AU Schulze, J.; Fink, C.; Sulima, T.; Eisele, I.; Hansch, W.
CS Institut fur Physik, Universitat der Bundeswehr Munchen, Neubiberg, 85577, Germany
SO Thin Solid Films (2000), 380(1,2), 154-157
CODEN: THSFAP; ISSN: 0040-6090
PB Elsevier Science S.A.
DT Journal
LA English
AB Tunneling devices are an interesting alternative to conventional MOS devices due to their high speed switching capabilities. Recently, it was shown that tunneling **transistors** based on **vertical** MOS-gated pin diodes can be fabricated. The pin diodes themselves were grown by means of UHV-MBE on highly n+-doped **Si**(100) substrates

with a 100-nm-thick **intrinsic** channel **region**. The top contact was formed by the deposition of a highly doped B δ-layer with a peak doping amount of approx. 1021 cm-3 for the necessary abrupt pn-junction and 300-nm p+-contact region. At a low supply voltage of -0.2 V, a current gain of three orders of magnitude with saturation behavior is achieved. In the present contribution, the authors have shown the influence of the amount of B in the δ-layer and of the abruptness of the drain-channel-junction on the transistor behavior. For that, they have discussed the characteristics of MOS-gated pin diodes on **Si** (111) with ultrasharp B δ's with a peak doping amount between 1020 and 1021 cm-3 and a peak width <3 nm, in comparison with MOS-gated pin diodes on **Si**(100) presented in W. Hansch et al. (2000). In order to obtain these highly doped ultra-sharp B δ-layers, a phase-transition from an elec. inactive **Si**(111)-√3+√3-R30° B surface phase into an elec. active one was induced by rapid thermal annealing.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(MOS-gated tunneling transistors in **Si**(100) and **Si** (111))
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 9 THERE ARE 9 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L37 ANSWER 5 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:783851 HCAPLUS
DN 132:8252
TI Method for selectively doping the intrinsic collector of an epitaxial base **vertical** bipolar **transistor**
IN Marty, Michel; Chantre, Alain; Schwartzmann, Thierry
PA STMicroelectronics S.A., Fr.; Commissariat A L'Energie Atomique; France Telecom
SO Eur. Pat. Appl., 13 pp.
CODEN: EPXXDW
DT Patent
LA French
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 962967	A1	19991208	EP 1999-401338	19990603
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	FR 2779571	A1	19991210	FR 1998-7060	19980605
	FR 2779571	B1	20030124		
	US 6265275	B1	20010724	US 1999-323525	19990601
	JP 11354537	A2	19991224	JP 1999-156065	19990603
PRAI	FR 1998-7060	A	19980605		

AB One effects selective doping of the collector by 1st implantation of dopants before epitaxy of the base and by 2nd implantation of dopants across the epitaxial base. One obtains 2 implanted zones of different widths. The base of the transistor is thinned and the collector resistance is optimized.

IT **7440-21-3, Silicon**, processes **11148-21-3**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(method for selectively doping **intrinsic** collector of epitaxial **base vertical** bipolar **transistor**
)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L37 ANSWER 6 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:706040 HCAPLUS
DN 129:297224
TI Vertical insulated gate field-effect transistor, method of making it and corresponding integrated circuit
IN Degawa, Toshihiko
PA Sharp Kabushiki Kaisha, Japan
SO Eur. Pat. Appl., 14 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 872895	A2	19981021	EP 1998-302765	19980408
	EP 872895	A3	19990224		
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 10290007	A2	19981027	JP 1997-96163	19970414
	TW 400649	B	20000801	TW 1998-87104285	19980323
	US 6215150	B1	20010410	US 1998-55214	19980406
PRAI	JP 1997-96163	A	19970414		

AB The invention relates to a semiconductor device, characterized in that a trench is formed in a **silicon** substrate, an element isolation film is formed on an inner surface of said trench, and a drain region, a channel region and a source region are arranged vertically in a region encircled by said element isolation film; and that a gate insulating film is formed **inside** of these **regions** and a gate electrode is formed on an inner side portion of said gate insulating film, while a drain electrode or source electrode is formed on an outer side portion of said gate insulating film.

L37 ANSWER 7 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1996:380254 HCAPLUS
DN 125:102368
TI Vertical double-diffused MOSFETs and power semiconductor device containing them
IN Yamamoto, Masanori
PA Nec Corporation, Japan
SO U.S., 35 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5521410	A	19960528	US 1994-215110	19940321
JP 06275838	A2	19940930	JP 1993-62209	19930322
JP 2910489	B2	19990623		

PRAI JP 1993-62209 19930322

AB In a vertical double-diffused MOSFET comprising a semiconductor substrate of a 1st conductivity type, an epitaxial layer of the 1st conductivity type, and a gate insulating layer, a gate electrode coats the gate insulating layer. The gate electrode has a plurality of polygonal windows and ≥1 slit-shaped window. Each polygonal window has a center positioned on 1 of the lattice points of a 2-dimensional square lattice comprising a plurality of unit cells. Each slit-shaped window is laid on a straight line connecting 2 centers of 2 polygonal windows which are obliquely adjacent to one another. A 1st insulating layer is formed on the upper surface of the gate electrode. Second insulating layers are formed on the side walls of the gate electrode. A base region of a 2nd conductivity type having a predetd. base junction depth is formed in the surface of the epitaxial layer. The base region is self-aligned to the polygonal windows and the slit-shaped window. A source region of the 1st conductivity type has a source junction shallower than the base junction. The source **region** has an **inner** edge self-aligned to both of the polygonal windows and the slit-shaped window and an inner edge spaced from the polygonal windows by a predetd. distance.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(vertical double-diffused MOSFETs containing)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 8 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1996:342372 HCAPLUS
DN 125:72972
TI Investigation of lateral and vertical profiles enhanced by implantation
AU Mineji, A.; Hamada, K.; Saito, S.
CS ULSI Device Dev. Lab., NEC Corp., Sagamihara, 229, Japan
SO Materials Research Society Symposium Proceedings (1996), 396(Ion-Solid Interactions for Materials Modification and Processing), 751-756
CODEN: MRSPDH; ISSN: 0272-9172
PB Materials Research Society
DT Journal

LA English
AB In shallow junction formation with junction depth below 0.1 μm, enhanced diffusion control is essential. The purpose of this paper is to investigate the B enhanced diffusion by point defects, introduced by high dose implantation with amorphization. **Ge** ions were implanted to induce amorphization **within** the S/D **region** of pMOS. These results were compare with that of the B enhanced diffusion by point defects, induced by **Si**+ implant with non-amorphization. These results suggest that the B enhanced diffusion in lateral profiles is much smaller, compared with that in vertical profiles, when point defects were introduced by amorphization.
IT **7440-21-3, Silicon**, processes **7440-56-4, Germanium**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(lateral and vertical profiles enhanced by implantation)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7440-56-4 HCAPLUS
CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

L37 ANSWER 9 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:593555 HCAPLUS
DN 121:193555
TI **Vertical** field-effect **transistor**
IN Yamada, Manabu; Takahashi, Yoshitomo
PA Nippon Electric Co, Japan
SO Jpn. Kokai Tokkyo Koho, 4 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 06177389	A2	19940624	JP 1992-326373	19921207
	JP 2917720	B2	19990712		
PRAI	JP 1992-326373		19921207		

AB The FET, comprising a conductive poly-**Si** gate electrode film formed on a surface (involving drain and source region) through a gate insulating film, comprises an insulating film which is thicker than that of an insulating film formed on **intrinsic** poly-**Si** **region** (arranged in the gate electrode center) and those of other insulating films (arranged on the **intrinsic** poly-**Si** **region**). The structure decreases gate electrode capacity.
IT **7440-21-3, Silicon**, uses
RL: PRP (Properties)
(polycryst., vertical FET gate electrode, structure for capacity decrease of)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 10 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:336957 HCAPLUS
DN 120:336957
TI Forming a **vertical transistor**
IN Malhi, Satwinder
PA Texas Instruments Inc., USA
SO U.S., 5 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5294559	A	19940315	US 1990-559756	19900730
	JP 04233764	A2	19920821	JP 1991-214437	19910730
	JP 3246753	B2	20020115		
	US 6194773	B1	20010227	US 1995-384816	19950206
PRAI	US 1990-559756	A	19900730		
	US 1994-187570	B1	19940126		

AB A **vertical transistor** comprises a semiconductor layer of a 1st conductivity type having a 1st doped region formed therein. A 2nd doped **region** is formed **within** the 1st doped **region**. A gate overlies the 1st doped region such that a low-impedance path between the 2nd doped region and the semiconductor layer may be created responsive to a voltage applied to the gate. Isolation regions are formed through the semiconductor layer to isolate the transistor from other devices.
IT **7440-21-3P, Silicon**, uses
RL: IMF (Industrial manufacture); PREP (Preparation)
(**vertical transistors** based on, manufacture of)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 11 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1994:21454 HCAPLUS
DN 120:21454
TI Vertical MOSFETs
IN Shinohara, Toshiaki; Kusuyama, Koichi
PA Nissan Motor, Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 05110105	A2	19930430	JP 1991-264927	19911014
	JP 2871232	B2	19990317		
PRAI	JP 1991-264927		19911014		

AB In a semiconductor device containing vertical MOSFETs which comprise a source region formed on the top side of a semiconductor substrate, a drain **region** formed **inside** or on the bottom side of the substrate, a channel region formed between the source and drain regions, and under the source region, and gate electrodes which sandwich the channel region across a gate-insulator film, the width of the channel region between gate electrodes is set shorter than that of the source-region top, and 1 end of the gate-insulator film in the channel region is inclined by a predetd. angle with respect to the substrate surface, while the other end is parallel with the 1st end. The MOSFETs have uniform characteristics.

IT **7440-21-3, Silicon**, uses
RL: USES (Uses)
(poly-, gate electrodes from, vertical MOSFETs containing, semiconductor devices containing)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 12 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1992:624565 HCAPLUS

DN 117:224565

TI Vertical-type insulated-gate field-effect transistors

IN Haneda, Hisashi

PA NEC Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04127574	A2	19920428	JP 1990-249096	19900919
PRAI	JP 1990-249096		19900919		

AB A vertical-type insulated-gate FET, which has a 2nd-conductivity-type base region in a 1st-conductivity-type semiconductor substrate, a 1st-conductivity-type source **region inside** the **base region**, a gate electrode from a 1st elec.-conductive film which is formed, across a gate-insulator film, on the exposed part of the substrate in the base region, and a 2nd elec.-conductive film above the 1st elec.-conductive film, which is connected with the source region across an insulator film, contains a highly resistive semiconductor film (e.g., poly-**Si**) on the 1st elec.-conductive film. Short circuiting of source and gate electrodes can be prevented.

IT **7440-21-3, Silicon**, uses
RL: PRP (Properties)
(polycryst., highly resistive films from, vertical-type FETs containing)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 13 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1991:645882 HCAPLUS
DN 115:245882
TI **Vertical** MOS field-effect **transistors** with increased breakdown voltage
IN Shigeta, Norihiro; Okada, Shigemi
PA Sanyo Electric Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 5 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
JP 03155167	A2	19910703	JP 1989-294702	19891113
PRAI JP 1989-294702		19891113		

AB A vertical MOSFET, which comprises a semiconductor substrate (common drain), a lattice-shaped diffusion layer, a source region in the surface of the diffusion layer, a gate electrode on an insulator-covered channel region between the source region and the substrate, and a source electrode in contact with both the source region and diffusion region, is characterized in that: the diffusion region is divided into the peripheral and **internal regions**; the source **region** is removed and in a floating state; and the source electrode is also in contact with the peripheral diffusion region. The MOSFET has increased breakdown voltage.
IT **7440-21-3, Silicon**, uses and miscellaneous
RL: USES (Uses)
(common drains from, vertical MOSFETs containing, with large breakdown voltage)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L37 ANSWER 14 OF 14 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1988:642397 HCAPLUS
DN 109:242397
TI Vertical-type metal-oxide-semiconductor field-effect transistor
IN Yao, Takeyuki
PA Nissan Motor Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	JP 63177473	A2	19880721	JP 1987-7753	19870116
	JP 2501810	B2	19960529		
PRAI	JP 1987-7753		19870116		

AB The FET comprises: a semiconductor substrate from a laminate of a low-resistivity region and a high-resistivity region; a base region which is formed in the high-resistivity region and has a conductivity type opposite to that of the latter; source regions which are formed in the base region and away from the substrate; and a polycryst. semiconductor (e.g., **Si**) **region inside** the **base region** and right below the source regions. The structure prevents the flow of a large elec. current which cannot be controlled by the gate potential.

IT **7440-21-3, Silicon**, uses and miscellaneous
RL: PRP (Properties)
(polycryst., vertical MOSFET containing region of, in base region)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

(FILE 'HOME' ENTERED AT 10:57:53 ON 26 FEB 2004)

FILE 'REGISTRY' ENTERED AT 10:59:42 ON 26 FEB 2004

L1 80 SEA ABB=ON PLU=ON SI/MF
L2 129 SEA ABB=ON PLU=ON GE/MF
L3 716 SEA ABB=ON PLU=ON GE.SI/MF OR GE SI/ELF

FILE 'HCAPLUS' ENTERED AT 11:00:07 ON 26 FEB 2004

L4 1234092 SEA ABB=ON PLU=ON L1 OR SILICON OR SI OR SILICA
L5 154122 SEA ABB=ON PLU=ON L2 OR GERMANIUM OR GE
L6 18378 SEA ABB=ON PLU=ON L3 OR SILICON(W)GERMANIUM OR SIGE
L7 1328628 SEA ABB=ON PLU=ON (L4 OR L5 OR L6)
L8 878 SEA ABB=ON PLU=ON L7 AND VERTICAL?(3A)(NPN OR PNP OR TRANSIST?)
L9 31 SEA ABB=ON PLU=ON L8 AND (PNP(3A)TRANSIST? AND NPN(3A)TRANSIST?)
L10 4 SEA ABB=ON PLU=ON L9 AND (BICMOS OR BIPOLAR(W)COMPLEMENTARY(W)METAL(W)OXIDE)

L11 27 SEA ABB=ON PLU=ON L9 NOT L10
L12 3 SEA ABB=ON PLU=ON L11 AND HIGH(3A)PERFORM?

L13 24 SEA ABB=ON PLU=ON L11 NOT L12
L14 4 SEA ABB=ON PLU=ON L13 AND (BASE OR REGION)(3A)(EXTRINSIC? OR EXTERNAL? OR OUTSIDE)

L15 20 SEA ABB=ON PLU=ON L13 NOT L14
L16 0 SEA ABB=ON PLU=ON L15 AND (INTRINSIC? OR INTERNAL? OR INNER? OR WITHIN OR INSIDE)(3A)REGION
L17 0 SEA ABB=ON PLU=ON L15 AND (CUTOFF OR CUT(W)OFF OR LIMIT?)(3A)(FREQUENC? OR GHZ OR GIGAHERTZ)
L18 1 SEA ABB=ON PLU=ON L15 AND MASK?

L19 19 SEA ABB=ON PLU=ON L15 NOT L18

L20 847 SEA ABB=ON PLU=ON L8 NOT L9
L21 14 SEA ABB=ON PLU=ON L20 AND (BASE OR REGION)(3A)(EXTRINSIC? OR EXTERNAL? OR OUTSIDE)
L22 3 SEA ABB=ON PLU=ON L21 AND (INTRINSIC? OR INTERNAL? OR INNER? OR WITHIN OR INSIDE)(3A)REGION

L23 11 SEA ABB=ON PLU=ON L21 NOT L22
L24 1 SEA ABB=ON PLU=ON L23 AND (CUTOFF OR CUT(W)OFF OR LIMIT?)(3A)(FREQUENC? OR GHZ OR GIGAHERTZ)

L25 10 SEA ABB=ON PLU=ON L23 NOT L24
L26 0 SEA ABB=ON PLU=ON L25 AND (RF OR RADIO(3A)FREQUENC? OR RADIOFREQUENC?)
L27 10 SEA ABB=ON PLU=ON L23 NOT L24

L28 833 SEA ABB=ON PLU=ON L20 NOT L21
L29 28 SEA ABB=ON PLU=ON L28 AND (INTRINSIC? OR INTERNAL? OR INNER? OR WITHIN OR INSIDE)(3A)(REGION OR BASE)
L30 0 SEA ABB=ON PLU=ON L29 AND (RF OR RADIO(3A)FREQUENC? OR RADIOFREQUENC?)
L31 6 SEA ABB=ON PLU=ON L29 AND MASK?

L32	22	SEA ABB=ON	PLU=ON	L29 NOT L31
L33	2	SEA ABB=ON	PLU=ON	L32 AND (P OR N)(1A)(TYPE OR EMIT?)
L34	20	SEA ABB=ON	PLU=ON	L32 NOT L33
L35	0	SEA ABB=ON	PLU=ON	L34 AND HIGH(3A)PERFORM?
L36	6	SEA ABB=ON	PLU=ON	L34 AND EMIT?
L37	14	SEA ABB=ON	PLU=ON	L34 NOT L36

L10 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:387646 HCAPLUS
DN 136:393050
TI **BiCMOS**-integrated photodetecting semiconductor device having an avalanche photodiode
IN Sahara, Masanori; Suzuki, Takashi
PA Hamamatsu Photonics K.K., Japan
SO U.S., 27 pp., Cont.-in-part of Appl. No. PCT/JP99/00397.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6392282	B1	20020521	US 2000-628446	20000728
	JP 11046010	A2	19990216	JP 1998-19302	19980130
	JP 11045988	A2	19990216	JP 1998-19311	19980130
	WO 9939391	A1	19990805	WO 1999-JP397	19990129

W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI JP 1998-19302 A 19980130
JP 1998-19311 A 19980130
WO 1999-JP397 A2 19990129
JP 1997-137023 A 19970527

AB **BiCMOS**-integrated photodetecting semiconductor devices are described which comprise an avalanche photodiode, a **vertical PNP transistor**, an N-channel MOS transistor for an N-channel MOS transistor, a P-channel MOS transistor for a P-channel MOS **transistor**, and a **vertical** type **NPN transistor** all formed on a P-type semiconductor substrate.
IT **7440-21-3**, **Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(**BiCMOS**-integrated photodetecting semiconductor device having avalanche photodiode)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D L10 BIB AB TOT HITSTR

L10 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:387646 HCAPLUS
DN 136:393050
TI **BiCMOS**-integrated photodetecting semiconductor device having an

avalanche photodiode
IN Sahara, Masanori; Suzuki, Takashi
PA Hamamatsu Photonics K.K., Japan
SO U.S., 27 pp., Cont.-in-part of Appl. No. PCT/JP99/00397.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 2

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6392282	B1	20020521	US 2000-628446	20000728
JP 11046010	A2	19990216	JP 1998-19302	19980130
JP 11045988	A2	19990216	JP 1998-19311	19980130
WO 9939391	A1	19990805	WO 1999-JP397	19990129

W: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IN, IS, KE, KG, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM
RW: GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG

PRAI JP 1998-19302 A 19980130
JP 1998-19311 A 19980130
WO 1999-JP397 A2 19990129
JP 1997-137023 A 19970527

AB **BiCMOS**-integrated photodetecting semiconductor devices are described which comprise an avalanche photodiode, a **vertical PNP transistor**, an N-channel MOS transistor for an N-channel MOS transistor, a P-channel MOS transistor for a P-channel MOS **transistor**, and a **vertical** type **NPN transistor** all formed on a P-type semiconductor substrate.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(**BiCMOS**-integrated photodetecting semiconductor device having avalanche photodiode)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:251894 HCAPLUS
DN 136:271757
TI High-voltage complementary bipolar and **BiCMOS** devices using double epitaxial growth
IN Hebert, Francois; Chen, Datong; Razouk, Reda
PA National Semiconductor Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6365447	B1	20020402	US 1998-5786	19980112
PRAI	US 1998-5786		19980112		

AB A method of making high-voltage complementary bipolar and **BiCMOS** devices on a common substrate. The bipolar devices are **vertical NPN** and **PNP transistors** having the same structure. The fabrication process utilizes trench isolation and thus is scalable. The process uses two epitaxial **silicon** layers to form the high-voltage NPN collector, with the PNP collector formed from a p-well diffused into the two epitaxial layers. The collector contact resistance is minimized by the use of sinker up/down structures formed at the interface of the two epitaxial layers. The process minimizes the thermal budget and therefore the up diffusion of the NPN and PNP buried layers. This maximizes the breakdown voltage at the collector-emitter junction for a given epitaxial thickness. The epitaxial layers may be doped as required depending upon the specifications for the high-voltage NPN device. The process is compatible with the fabrication of low-voltage devices, which can be formed by placing the sinker regions under the emitter region. The thicknesses of the two epitaxial layers may be adjusted as required depending upon the specifications for the low-voltage devices.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(high-voltage complementary bipolar and **BiCMOS** devices using double epitaxial growth)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 2000:589122 HCAPLUS

DN 133:328044

TI The piezojunction effect in **NPN** and **PNP vertical transistors** and its influence on **silicon** temperature sensors

AU Fruett, F.; Wang, G.; Meijer, G. C. M.

CS Electronics Research Laboratory, Delft University of Technology, Delft, 2628 CD, Neth.

SO Sensors and Actuators, A: Physical (2000), A85(1-3), 70-74
CODEN: SAAPEB; ISSN: 0924-4247

PB Elsevier Science S.A.

DT Journal

LA English

AB This paper describes a test structure to characterize the piezojunction effect for the base-emitter voltage VBE and the PTAT voltage ΔVBE. The piezojunction effect directly affects the accuracy of temperature sensors and special types of pressure sensors. Packaging is a source of mech. stress in electronics circuits. Measurements have been performed for two types of **vertical** bipolar **transistors**. Firstly, an **NPN transistor** of a **BiCMOS** technol. and secondly, a **PNP** substrate **transistor** of a CMOS

technol., both of them using a [100] **silicon** wafer geometry. It has been found that the sensitivity for the uniaxial stress of the VBE of the PNP is four times less than that of the **NPN transistor**. In both cases, the PTAT voltage appears to be hardly stress-sensitive.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L10 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:508177 HCAPLUS
DN 133:98153
TI Method for making high gain lateral **PNP** and **NPN** bipolar **transistor** compatible with CMOS for making **BiCMOS** circuits
IN Verma, Purakh Raj; Kuek, Joe Jin
PA Chartered Semiconductor Manufacturing, Ltd., Singapore
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6093613	A	20000725	US 1998-20496	19980209
	SG 71812	A1	20000418	SG 1998-1559	19980630
	US 6249031	B1	20010619	US 2000-534551	20000327
PRAI	US 1998-20496	A	19980209		

AB A method and lateral bipolar transistor structure are achieved, with high current gain, compatible with CMOS processing to form **BiCMOS** circuits. Making a lateral PNP bipolar involves forming an n- well in a p- doped **Si** substrate. A patterned Si3N4 layer was used as an oxidation barrier mask to form field oxide isolation around device areas by the LOCOS method. A polysilicon layer over device areas is patterned to leave portions over the intrinsic base areas of the L-PNP bipolar an implant block-out mask. A buried N- base region is implanted in the substrate under the emitter region. A photoresist mask and the patterned polysilicon layer were used to implant the p++ doped emitter and collector for the L-PNP. The emitter junction depth xj intersects the highly doped n+ buried base region. This n+ doped base under the emitter reduces the current gain of the unwanted (parasitic) **vertical PNP** portion of the L-PNP bipolar to reduce the current gain of the V-PNP. The built-in potential Vbi of the emitter-base junction also increases further the current gain of the V-PNP thereby increasing the gain of the L-**PNP** bipolar **transistor**. By reversing the polarity of the dopants, L-NPN components can also be made. Also by implanting a tetravalent impurity such as **Ge**, **Si**, or C, the current gain of the L-PNP can be further improved.

IT **7440-56-4**, **Germanium**, uses
RL: MOA (Modifier or additive use); USES (Uses)
(in method for making high gain lateral **pnp** and **npn** bipolar **transistor** compatible with CMOS for making **BiCMOS** circuits)
RN 7440-56-4 HCAPLUS
CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT **7440-21-3D, Silicon**, ions, processes **7440-56-4D**
, Germanium, ions, processes
RL: NUU (Other use, unclassified); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(in method for making high gain lateral **pnp** and **npn** bipolar **transistor** compatible with CMOS for making **BiCMOS** circuits)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 7440-56-4 HCAPLUS
CN Germanium (7CI, 8CI, 9CI) (CA INDEX NAME)

Ge

IT **7440-21-3P, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); SPN (Synthetic preparation); PREP (Preparation); PROC (Process); USES (Uses)
(method for making high gain lateral **pnp** and **npn** bipolar **transistor** compatible with CMOS for making **BiCMOS** circuits)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 1 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:850549 HCAPLUS
DN 136:93842
TI A complementary bipolar technology family with a **vertically** integrated **PNP** for high-frequency analog applications
AU Bashir, Rashid; Hebert, Francois; DeSantis, Joseph; McGregor, Joel M.; Yindeepol, Wipawan; Brown, Kevin; Moraveji, Farhood; Mills, Thomas B.; Sadovnikov, Alexei; McGinty, James; Hopper, Peter; Sabsowitz, Robert; Khidr, Mohamed; Krakowski, Tracey; Smith, Linda; Razouk, Reda
CS School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN, 47907, USA
SO IEEE Transactions on Electron Devices (2001), 48(11), 2525-2534
CODEN: IETDAI; ISSN: 0018-9383
PB Institute of Electrical and Electronics Engineers
DT Journal; General Review
LA English
AB A review. **Silicon** complementary bipolar processes offer the possibility of realizing **high-performance** circuits for a variety of analog applications. This paper presents a summary of **silicon** complementary bipolar process technol. reported in recent years. Specifically, an overview of a family of **silicon** complementary bipolar process technologies, called **Vertically** Integrated **PNP** (VIP), which have been used for the realization of high-frequency analog circuits is presented. Three process technologies, termed VIP-3, VIP-3H, and VIP-4H offer device breakdowns of 40, 85, and 170 V, resp. These processes feature optimized **vertically** integrated bipolar junction **transistors** (**PNPs**) along with **high performance NPN transistors** with polycryst. **silicon** emitters, low parasitic polycryst. **silicon** resistors, and metal-insulator-polycryst. **silicon** capacitors. Key issues and aspects of the processes are described. These issues include the polycryst. **silicon** emitter optimization and vertical and lateral device isolation in the transistors. Circuit design examples are also described which have been implemented in these technologies.
IT **7440-21-3**, **Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(complementary bipolar technol. family with a **vertically** integrated **PNP** for high-frequency analog applications)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 62 THERE ARE 62 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L12 ANSWER 2 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1982:44849 HCAPLUS
DN 96:44849
TI **High performance PNP** and **NPN transistor** structure
IN Horng, Cheng Tzong; Konian, Richard Robert; Schwenker, Robert Otto; Wieder, Armin Wilhelm
PA International Business Machines Corp. , USA

SO Eur. Pat. Appl., 37 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 39411	A2	19811111	EP 1981-102499	19810402
R: DE, FR, GB, IT				
CA 1148269	A1	19830614	CA 1981-372670	19810310
US 4378630	A	19830405	US 1981-309627	19811008
PRAI US 1980-146921		19800505		

AB The structure provides **vertical npn** and lateral **pnp transistors** within the same semiconductor chip. The base of the **pnp transistor** is very narrow (.apprx.300-400 nm), obtained in part by using a well-defined chemical vapor-deposited oxide mask instead of conventional lithog. masking. To eliminate the emitter current injected into the substrate, the p+ emitter and p+ collector of the **pnp transistor** are bonded by Si3N4 and SiO2 layers.

L12 ANSWER 3 OF 3 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1970:460533 HCAPLUS
DN 73:60533
TI Field effect transistors for integrated circuits
IN Kronlage, John W.
PA Texas Instruments Inc.
SO S. African, 33 pp.
CODEN: SFXXAB
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI ZA 6904664		19700119		
GB 1278281			GB	
PRAI US		19680829		

AB **High**-quality and **high-performance** p-channel field-effect transistors [FET] having low noise figures are fabricated as devices per se or in an integrated circuit including a complementary n-channel FET and (or) **vertical** and surface bipolar **npn** and **pnp transistors** and resistors, all formed on the same monolithic chip or slice. The use of p-channel FETs in such integrated circuits permits addnl. design flexibility and optimum circuit performance. The complementary n- and p-channel transistors may be used to fabricate differential/operational amplifiers having high gain, low noise, high output voltage swing, and balanced amplifier stages. Thus, to form a p-channel FET: (1) a 1st p-type, B-doped region is diffused into the surface of an n-type, P-doped, single-crystal **Si** substrate; (2) then, a 1st n+-type region, Sb- or As-doped, is diffused into the 1st p-type region, forming a back gate for the p-channel transistor; (3) an n-type epitaxial layer is formed over the surface by thermal decomposition of trichlorosilane in a H atmospheric containing a few ppm arsine; (4) a lightly B-doped p-type region is formed by diffusion into the surface of the epitaxial layer, thus forming the channel region; (5) a B-doped p+ barrier or isolation ring is formed around the periphery and contacting the 1st p-type region, thus providing effective isolation from the n-type

substrate by reverse biasing; (6) p-type source and drain regions and an n+ front gate region are formed by diffusion on the surface of the p-type layer. n-Channel FET and bipolar **npn** and **pnp** **transistors** may be formed concurrently on the same substrate as desired for use in an integrated circuit.

L14 ANSWER 1 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:203348 HCAPLUS
DN 138:213790
TI Manufacturing method of a semiconductor device having a polysilicon electrode
IN Kim, Jong-hwan; Kim, Cheol-joong; Lee, Suk-kyun; Choi, Yongcheol
PA Fairchild Korea Semiconductor Ltd., S. Korea
SO U.S. Pat. Appl. Publ., 31 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2003049909	A1	20030313	US 2002-94445	20020308
PRAI KR 2001-56518	A	20010913		

AB A semiconductor device and a method of manufacturing the semiconductor device having a **vertical NPN** bipolar **transistor**, a lateral **PNP** bipolar **transistor**, and P-type and N-type resistors are disclosed which are manufactured in a reduced number of steps. In one embodiment, a photoresist pattern is formed on a pad oxide layer and field oxides on an N-type epitaxial layer that is grown on a P-type semiconductor substrate. The pad oxide layer is etched after implanting P-type impurity into the epitaxial layer by using the photoresist pattern as a mask. Deposition of a polysilicon layer after removing the photoresist pattern is followed by implanting P-type impurity and N-type impurity into the polysilicon layer in sequence. Another photoresist pattern formed on the polysilicon layer after the previous implantation was used as an etch mask for etching the polysilicon layer to form polysilicon electrodes of transistors and P-type and N-type resistors as well as expose the surface of the epitaxial layer near an emitter region of the **vertical transistor**. P-type impurity is implanted into the epitaxial layer through the exposed surface thereof by using the photoresist pattern as an implant mask. The structure is then subjected to heat treatment to form emitter, intrinsic and **extrinsic base**, and collector **regions** of the transistors.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PYP (Physical process); PROC (Process); USES (Uses)
(poly-; manufacturing semiconductor device having polysilicon electrode)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L14 ANSWER 2 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2002:444559 HCAPLUS
DN 137:14465
TI Complementary **vertical** bipolar-junction **transistors** fabricated in **silicon**-on-sapphire substrate utilizing wide base **PNP transistors**
IN Cartagena, Eric N.

PA United States Dept. of the Navy, USA
SO U.S., 22 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 6404038	B1	20020611	US 2000-517292	20000302
US 2000-517292		20000302		

AB A method for fabricating complementary **vertical** bipolar junction **transistors** of **silicon**-on-sapphire in fewer steps than required for true complimentary **vertical** bipolar junction **transistors** is disclosed. Initially a thin layer of **silicon** is grown on a sapphire substrate. The **silicon** is improved using double solid phase epitaxy. The **silicon** is then patterned and implanted with P+-type and N+-type dopants. Subsequently a micrometer scale N-type layer is grown that acts as the intrinsic base for both an **PNP transistor** and as the collector for an **NPN transistor**. The **extrinsic base** for the NPN is then formed and the emitter, collector and ohmic contact regions are next selectively masked and implanted. Conductive metal is then formed between protecting oxide to complete the complementary **vertical** bipolar junction **transistors**.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(complementary **vertical** bipolar junction **transistors** fabricated in **silicon**-on-sapphire substrate utilizing wide base **PNP transistors**)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 23 THERE ARE 23 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L14 ANSWER 3 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:763809 HCAPLUS
DN 132:8198
TI Method of making an integrated **vertical** bipolar **transistor**
IN Yoshida, Hiroshi
PA NEC Corporation, Japan
SO Eur. Pat. Appl., 19 pp.
CODEN: EPXXDW
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
EP 961316	A2	19991201	EP 1999-110147	19990525
EP 961316	A3	20030625		

R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO

	JP 11340335	A2	19991210	JP 1998-144316	19980526
	JP 3252898	B2	20020204		
	US 6337252	B1	20020108	US 1999-315826	19990521
PRAI	JP 1998-144316	A	19980526		

AB There is provided a method of manufacturing a semiconductor device which can use commonly a part of a step of forming a **PNP transistor** with a step of forming an **NPN transistor**. In an area isolated by a later isolation region of PNP formed by doping N-type impurities simultaneously with the formation of the collector region of NPN, an N-type bottom isolation region of PNP, a collector region, and a base region are formed by using the same mask. Trenches extending to the collector regions are formed by an overetching treatment carried out when the emitter electrodes of PNP and NPN are subjected to a patterning treatment, and N-type impurities are doped through the trench simultaneously with the formation of an **external base region** of PNP, thereby forming a collector drawing region of NPN. Further, P-type impurities are doped through the trench simultaneously with the formation of an **external base region** of NPN, thereby forming a collector drawing region of PNP.

IT **7440-21-3**, **Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of integrated **vertical** bipolar **transistors** based on)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L14 ANSWER 4 OF 4 HCAPLUS COPYRIGHT 2004 ACS on STN

AN 1998:242235 HCAPLUS

DN 128:303016

TI Complementary bipolar transistors, integrated injection logic circuits and semiconductor devices using them, and their production

IN Kim, Jong-Hwan; Kim, Cheol-Joong; Kwon, Tae-Hoon; Lee, Suk-Kyun

PA Samsung Electronics Co., Ltd., S. Korea

SO Ger. Offen., 114 pp.
CODEN: GWXXBX

DT Patent

LA German

FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	DE 19744860	A1	19980416	DE 1997-19744860	19971010
	CN 1179627	A	19980422	CN 1997-119313	19971010
	US 6326674	B1	20011204	US 1999-451623	19991130
	US 2002017703	A1	20020214	US 2001-978521	20011016
	US 6573146	B2	20030603		
PRAI	KR 1996-46600	A	19960910		
	KR 1996-45305	A	19961011		
	KR 1997-46600	A	19970910		
	US 1997-949223	A3	19971010		
	US 1999-451623	A3	19991130		

AB The complementary bipolar **transistor** comprises a lateral

npn bipolar **transistor**, **vertical** and lateral **pnp transistors**, an integrated injection logic circuit, a diffusion capacitor, a polysilicon capacitor, and polysilicon resistors. The lateral **pnp transistor** has emitter and collector regions which include high- and low-d. regions, and the emitter region is formed in an n-type trench region. In the integrated injection logic circuit, collector regions are surrounded by high-d. p-type regions and low-d. p-type regions are formed under the collector regions. The diffusion and polysilicon capacitors are formed in the substrate. The diffusion **regions outside** the **regions** formed by diffusion of the impurities in the polysilicon resistors into the epitaxial layer are formed before the formation of the polysilicon resistors, and the polysilicon electrodes are formed together with the polysilicon resistors.

IT **7440-21-3**, **Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; manufacture of complementary bipolar transistors containing)

RN 7440-21-3 HCAPLUS

CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L18 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:551445 HCAPLUS
DN 133:170999
TI Fabrication of bipolar CMOS semiconductor device having **vertical pnp** and **npn transistors**
IN Yoshida, Hiroshi
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000223601	A2	20000811	JP 1999-22514	19990129
	JP 3216716	B2	20011009		
PRAI	JP 1999-22514		19990129		

AB The title method involves forming a field oxide film on a p-type **Si** substrate, forming a first oxide film, forming gate electrodes and a polysilicon layer containing an oxide film(s) as a **mask** for forming the pnp-forming region having an ion-implanted emitter structure, forming a second oxide film on the overall substrate including the gate electrodes and **mask**, removing the first and second oxide films at the regions for forming collector and emitter contacts and removing the polysilicon layer at the pnp emitter contact in patterning the polysilicon layer as well as etching the **silicon** at the npn and pnp collectors. The number of fabrication steps and device size are decreased.

IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(fabrication of bipolar CMOS semiconductor device having **vertical pnp** and **npn transistors**)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 1 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:777009 HCAPLUS
DN 139:269247
TI Design and fabrication of a semiconductor device having high-speed PNP and **NPN** heterojunction bipolar **transistors**
IN Ikeda, Tatsuhiko
PA Japan
SO U.S. Pat. Appl. Publ., 28 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003183903	A1	20031002	US 2002-246406	20020919
	JP 2003297843	A2	20031017	JP 2002-92622	20020328
PRAI	JP 2002-92622	A	20020328		

AB The invention relates to the design and fabrication of a semiconductor device having high-speed PNP and **NPN** heterojunction bipolar **transistors** formed on a single substrate. The semiconductor device consists of a **vertical NPN** bipolar **transistor** and a **vertical PNP** bipolar **transistor**, each having a collector layer, a base layer, and an emitter layer formed on a common **silicon** substrate. Each of the **vertical NPN** bipolar **transistor** and the **vertical PNP** bipolar **transistor** consists of (i) a first epitaxial layer formed on the surface of the **silicon** substrate; (ii) an isolation insulating film disposed on the surface of the first epitaxial layer; (iii) a first portion of the collector layer formed on the surface of the first epitaxial layer and surrounded by the isolation insulating film; and (iv) a second epitaxial layer extending on the first epitaxial layer and the isolation insulating film, where the second epitaxial layer consists of a **silicon** layer as a second portion of the collector layer, a **silicon germanium** layer as the base layer, and a **silicon** layer as the emitter layer in the order from the bottom.

IT **7440-21-3**, **Silicon**, uses **11148-21-3**
RL: DEV (Device component use); USES (Uses)
(design and fabrication of semiconductor device having high-speed PNP and **NPN** heterojunction bipolar **transistors**)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L19 ANSWER 2 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2003:203090 HCAPLUS
DN 138:213764
TI Electrostatic discharge protection **silicon** controlled rectifier for **silicon-germanium** technologies
IN Russ, Cornelius Christian; Armer, John; Mergens, Markus Paul Josef; Jozwiak, Phillip Czeslaw
PA Sarnoff Corporation, USA
SO U.S. Pat. Appl. Publ., 21 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2003047750	A1	20030313	US 2002-238699	20020910
	EP 1294025	A2	20030319	EP 2002-256293	20020911
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, SK				
	JP 2003179150	A2	20030627	JP 2002-265936	20020911
PRAI	US 2001-318550P	P	20010911		
	US 2002-238699	A	20020910		

AB An electrostatic discharge (ESD) protection device having a **Si** controlled rectifier (SCR) for protecting circuitry of an integrated circuit (IC) is prepared which is not as subject to failure as the prior art. The SCR includes a N-doped layer disposed over a substrate and a 1st P doped region disposed over the N-doped layer. At least one 1st N+ doped region forming a cathode is disposed over the P-doped region and coupled to ground. The at least one 1st N+ doped region, 1st P-doped region, and N-doped layer form a **vertical NPN transistor** of the SCR. A 2nd P doped region forming an anode is coupled to a protected pad. The 2nd P doped region is disposed over the N-doped layer, and is laterally positioned and elec. isolated with respect to the 1st P doped region. The 2nd P doped region, N-doped layer, and 1st P doped region form a lateral **PNP transistor** of the SCR.

IT **7440-21-3, Silicon,** uses **11148-21-3**
RL: DEV (Device component use); USES (Uses)
(electrostatic discharge protection **silicon** controlled rectifier for **silicon-germanium** technologies)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 11148-21-3 HCAPLUS
CN Germanium alloy, nonbase, Ge,Si (9CI) (CA INDEX NAME)

Component	Component Registry Number
Ge	7440-56-4
Si	7440-21-3

L19 ANSWER 3 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2001:598374 HCAPLUS

DN 135:161115
TI **Vertical** bipolar **transistor** based on gate induced drain leakage current which is compatible with CMOS fabrication processes
IN Chi, Min-Hwa; Jeng, Min-Chie
PA Taiwan
SO U.S. Pat. Appl. Publ., 7 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001013610	A1	20010816	US 1999-365436	19990802
	TW 447131	B	20010721	TW 2000-89100624	20000117
PRAI	US 1999-365436	A	19990802		

AB A **vertical npn** bipolar **transistor** formed in a p-type substrate is disclosed. The transistor comprises: a deep n-well formed within the p-type substrate; a buried n+ layer formed within the deep n-well; a p-well formed within the deep n-well and atop the buried n+ layer; an isolation structure surrounding the p-well and extending from the surface of the substrate to below the level of the p-well; a n+ structure formed within the p-well; and a gate formed above the p-well, the gate separated from the substrate by a thin oxide layer, the gate extending over at least a portion of the n+ structure. To turn on the **npn** bipolar **transistor**, the gate is pulsed to 0 V (or lower), generating GIDL current at the n+ structure and flowing into the p-well (as base current). A corresponding **vertical** gated **pnp** bipolar **transistor** can also be formed and operated similarly with reverse polarity of charge carriers and biases.
IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(**vertical** bipolar **transistor** based on gate induced drain leakage current which is compatible with CMOS fabrication processes)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 4 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 2000:259043 HCAPLUS
DN 132:287417
TI Semiconductor devices having **npn/pnp-transistors** on a SOI wafer and fabrication thereof
IN Sugiyama, Mitsuhiro
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 9 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000114391	A2	20000421	JP 1998-282134	19981005
	JP 3175707	B2	20010611		

PRAI JP 1998-282134 19981005
AB The title semiconductor devices have a **vertical npn-transistor** and a horizontal **pnp-transistor** provided across an isolation region on a substrate. The transistors are provided across a buried SiO2 film on the substrate, wherein a p+-layer of the horizontal **pnp-transistor** is provided in proximity to the SiO2 film. The buried **Si** oxide film gives the devices a stable base region width and consequently provides a stable lineality on the current amplification ratio regardless of an increase of collector current. The devices may be well applicable to communication bipolar ICs.
IT **7440-21-3, Silicon**, properties
RL: DEV (Device component use); PRP (Properties); USES (Uses)
(semiconductor devices having **npn/pnp-transistors** on a SOI wafer and fabrication thereof)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 5 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1999:468151 HCAPLUS
DN 131:96144
TI Complementary **Si/Si-Ge** heterojunction bipolar transistor fabrication
IN Bashir, Rashid; Hebert, Francois
PA National Semiconductor Corporation, USA
SO U.S., 11 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5930635	A	19990727	US 1997-850610	19970502
PRAI	US 1997-850610		19970502		

AB A method of manufacturing truly complementary bipolar transistors on a common substrate. The method results in the fabrication of **vertical NPN** and **PNP transistors** which have an identical structure and mode of operation, with both devices operating in the downward direction. The inventive method permits independent control of the characteristics of the two devices, producing a closely matched performance for both devices.
IT **7440-21-3, Silicon**, processes **12790-21-5**
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(complementary **silicon/silicon-germanium** heterojunction bipolar transistor fabrication)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RN 12790-21-5 HCAPLUS

CN Silicon alloy, base, Si,Ge (9CI) (CA INDEX NAME)

Component	Component Registry Number
Si	7440-21-3
Ge	7440-56-4

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 6 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:594653 HCAPLUS
DN 129:284473
TI Semiconductor devices and manufacturing thereof
IN Kuranochi, Atsushi
PA Sony Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10242291	A2	19980911	JP 1997-45873	19970228
PRAI JP 1997-45873		19970228		

AB The device has SiCx films (e.g., 0.5-5 nm thick) between a polycryst. **Si** emitter electrode and the emitter layer of a npn- and a **pnp**-bipolar **transistor** (e.g., double polycryst. **Si** bipolar **transistor** and **vertical** bipolar **transistor** type, resp.). The title process comprises formation of SiCx films on the base layers, deposition of polycryst. **Si** films to be formed to the emitter electrodes, ion implantation of a p- and an n-type impurity into the polycryst. **Si** films, (1) patterning of the polycryst. **Si** films to the emitter electrodes and heat treatment for diffusion of the p-type impurity to the surface of the base layer forming the emitter layer, and (2) heat treatment for diffusion of the n-type impurity onto the surface of the base layer forming the emitter layer and patterning of the polycryst. **Si** film to the emitter electrode, for the pnp- and the **npn**-bipolar **transistor**, resp. Current amplification factor is raised with increased emitter injection effect with decreased deviations of the current amplification factor and the base-emitter voltage.

IT **7440-21-3, Silicon**, properties
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PRP (Properties); PROC (Process); USES (Uses)
(polycryst., emitter electrode; semiconductor devices and manufacturing thereof)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 7 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:501244 HCAPLUS

DN 129:143792
TI **Vertical pnp transistor**, integrated circuit containing it, and fabrication of the transistor and the circuit
IN Lachner, Rudolf; Bianco, Michael
PA Siemens A.-G., Germany
SO Eur. Pat. Appl., 11 pp.
CODEN: EPXXDW
DT Patent
LA German
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI EP 855747	A1	19980729	EP 1998-100638	19980115
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
DE 19702320	A1	19980730	DE 1997-19702320	19970123
JP 10214846	A2	19980811	JP 1998-23911	19980121
PRAI DE 1997-19702320		19970123		

AB The base contact of the transistor, preferably of n-type polysilicon, is formed after the p-type polysilicon emitter contact, and thus is at least partially above the emitter contact. On integration with a **vertical npn transistor**, the emitter contact of the **pnp transistor** and the base contact of the **npn transistor** are formed from the same p-type polysilicon layer. The **pnp transistor** requires little space and is simple to fabricate.
IT **7440-21-3, Silicon**, processes
RL: DEV (Device component use); PEP (Physical, engineering or chemical process); PROC (Process); USES (Uses)
(polycryst.; fabrication of polysilicon base and emitter contacts in **vertical pnp transistor** for integrated circuits)
RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 8 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:334180 HCAPLUS
DN 129:61597
TI Manufacture of semiconductor devices with **NPN** and **PNP** **transistors**
IN Nagayama, Masanori
PA Hitachi Electronics Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 3 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI JP 10135235	A2	19980522	JP 1996-292414	19961105
PRAI JP 1996-292414		19961105		

AB N-type epitaxial layers are formed on the buried regions of **vertical NPN transistors**, device-isolation regions are formed, collector contact regions are etched away, and replaced by high-concentration P-type poly-**Si**, and base and emitter regions are formed. The **NPN transistors** have reduced collector contact resistance.

IT **7440-21-3, Silicon**, uses
RL: DEV (Device component use); USES (Uses)
(polycryst.; manufacture of semiconductor devices with **NPN** and **PNP transistors** with reduced collector contact resistance)

RN 7440-21-3 HCAPLUS
CN Silicon (7CI, 8CI, 9CI) (CA INDEX NAME)

Si

L19 ANSWER 9 OF 19 HCAPLUS COPYRIGHT 2004 ACS on STN
AN 1998:163313 HCAPLUS
DN 128:224835
TI Manufacture of semiconductor devices
IN Iwamoto, Yasuhiko
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 8 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 10070194	A2	19980310	JP 1996-226579	19960828
	JP 2907141	B2	19990621		
PRAI	JP 1996-226579		19960828		

AB The title process comprises sequential formation of 2nd conductivity type 1st regions for separation of **vertical pnp transistors** and 2nd conductivity type 2nd regions for high concentration collectors of **npn transistors** on a 1st conductivity type semiconductor substrate; 1st conductivity type 1st regions for **vertical pnp transistors** in the 2nd conductivity type 1st regions, a 1st conductivity type 2nd regions in the 2nd conductivity type 2nd regions, and a 2nd conductivity type 3rd regions in the 1st conductivity type regions; insulating layer(s) on the entire surface including the 1st conductivity type 2nd and the 2nd conductivity type 3rd regions; formation of contact holes in the insulating layer(s) over the 1st conductivity type 2nd and the 2nd conductivity type 3rd regions; and selective deposition of polycryst. **Si** film doped with a 2nd conductivity type impurity in the contact holes; doping of the 2nd conductivity type **Si** film in the contact holes over the 2nd conductivity type 3rd regions with a 1st conductivity type impurity converting the **Si** film to the 1st conductivity type; and formation of 2nd conductivity type 4th and 1st conductivity type 3rd regions in the 1st conductivity type 2nd and the 2nd conductivity

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 26feb04 09:40:55 User267149 Session D1259.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC  1969-2004/Feb W3
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request.  See HELP RATES 34.
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request.  See HELP RATES434.
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         (c)2004 Japan Science and Tech Corp(JST)
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         (c) 2004 The HW Wilson Co.
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         (c) 2004 Royal Soc Chemistry
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removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs  1970-2004/Jan
         (c) 2004 DECHEMA
  File 350:Derwent WPIX  1963-2004/UD,UM &UP=200413
         (c) 2004  Thomson Derwent
*File 350: New prices as of 1-1-04 per Information Provider request.
See HELP RATES350
  File 347:JAPIO  Oct 1976-2003/Oct(Updated 040202)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs  Aug 1985-2003/Nov
         (c) 2003 European Patent Office
  File 371:French Patents  1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set	Items	Description
S1	3846	AU=(GRAY, P? OR GRAY P?)
S2	28819	AU=(JOHNSON, J? OR JOHNSON J?)
S3	3	S1 AND S2
S4	3	RD (unique items)
S5	32662	S1:S2
S6	7	S5 AND VERTICAL?(3N)(NPN OR PNP OR TRANSIST?)
S7	7	S6 NOT S3
S8	4	RD (unique items)
S9	32652	S5 NOT S6,S4
S10	49	S9 AND (BICMOS OR BIPOLAR()COMPLEMENTARY()METAL()OXIDE)
S11	31	S10 AND (SILICON OR SI OR GERMANIUM OR GE OR SILICON()GERM-ANIUM OR SIGE)
S12	1	S11 AND (P OR N)(1N)(TYPE? ? OR EMIT??????)
S13	30	S11 NOT S12
S14	1	S13 AND BASE???(3N)(EXTRINSIC? OR EXTERNAL? OR OUTSIDE)
S15	29	S13 NOT S14
S16	2	S15 AND (CUTOFF OR CUT()OFF OR LIMIT??????)(3N)(FREQUENC? OR GHZ OR GIGAHERTZ)
S17	1	RD (unique items)
S18	27	S15 NOT S16
S19	15	RD (unique items)

4/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7176093 INSPEC Abstract Number: B2002-03-2570K-002
Title: A 0.18 mu m BiCMOS technology featuring 120/100 GHz (f/sub T//f/sub max/) HBT and ASIC-compatible CMOS using copper interconnect
Author(s): Joseph, A.; Coolbaugh, D.; Zierak, M.; Wuthrich, R.; Geiss, P.; He, Z.; Liu, X.; Orner, B.; **Johnson, J.**; Freeman, G.; Ahlgren, D.; Jagannathan, B.; Lanzerotti, L.; Ramachandran, V.; Malinowski, J.; Chen, H.; Chu, J.; **Gray, P.**; Johnson, R.; Dunn, J.; Subbanna, S.; Schonenberg, K.; Harame, D.; Groves, R.; Watson, K.; Jadus, D.; Meghelli, M.; Rylyakov, A.
Author Affiliation: Microelectron. Div., IBM Corp., Essex Junction, VT, USA
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.01CH37212) p.143-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 199 pp.
ISBN: 0 7803 7019 8 Material Identity Number: XX-2001-02296
U.S. Copyright Clearance Center Code: 0-7803-7019-8/01/$10.00
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron. Devices Soc.; IEEE Solid-State Circuits Soc.; IEEE Twin Cities Sect
Conference Date: 30 Sept.-2 Oct. 2001 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: A BiCMOS technology is presented that integrates a high performance NPN (f/sub T/=120 GHz and f/sub max/=100 GHz), ASIC compatible 0.11 mu m L/sub eff/ CMOS, and a full suite of passive elements. Significant HBT performance enhancement compared to previously published results has been achieved through further collector and base profile optimization guided by process and device simulations. Base transit time reduction was achieved by simultaneously increasing the Ge ramp and by limiting the base diffusion with the addition of carbon doping to SiGe epitaxial base. This paper describes IBM's next generation SiGe BiCMOS production technology targeted at the communications market.
Subfile: B

4/3,AB/2 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

03392936 INSIDE CONFERENCE ITEM ID: CN035824443
Increasing the Flexibility of Modelling Tools via Constraint-Based Specification
Gray, P.; Welland, R.
CONFERENCE: CASCON 1999-Conference (Meeting of minds)
P: 161-172
CASCON, 1999
LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE EDITOR(S): MacKay, S. A.; **Johnson, J. H.**
CONFERENCE SPONSOR: Consortium for Software Engineering Research
IBM TJ Watson Research Center
CONFERENCE LOCATION: Mississauga, Canada
CONFERENCE DATE: Nov 1999 (199911) (199911)
NOTE:

8/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7508997 INSPEC Abstract Number: B2003-02-2560J-018
Title: A simulation study on thin SOI bipolar transistors with fully or partially depleted collector
Author(s): Ouyang, Q.C.; Jin Cai; Tak Ning; Oldiges, P.; **Johnson, J.B.**
Author Affiliation: IBM Semicond. Res. & Dev. Center (SRDC), IBM T. J. Watson Res. Center, Yorktown Heights, NY, USA
Conference Title: Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No.02CH37384) p.28-31
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA 241 pp.
ISBN: 0 7803 7561 0 Material Identity Number: XX-2002-02195
U.S. Copyright Clearance Center Code: 0-7803-7561-0/02/$17.00
Conference Title: 2002 IEEE Bipolar/BICMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Solid-State Circuits Soc
Conference Date: 29 Sept.-1 Oct. 2002 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: **Vertical npn** BJTs on thin SOI with a partially or fully depleted collector are studied by 2-dimensional device simulations. It is found that compared to conventional bulk BJTs, the SOI BJTs have a reduced base-collector capacitance, a higher Early voltage and a higher breakdown voltage. A SOI BJT with a fully-depleted collector can achieve a higher f/sub max/ with a comparable current gain and f/sub T/.
Subfile: B

8/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

04200596 INSPEC Abstract Number: B9209-2560J-016
Title: A self-aligned short process for insulated-gate bipolar transistors
Author(s): Chow, T.P.; Baliga, B.J.; **Gray, P.V.**; Adler, M.S.; Chang, M.F.; Pifer, G.C.; Yilmaz, H.
Author Affiliation: General Electric Co., Schenectady, NY, USA
Journal: IEEE Transactions on Electron Devices vol.39, no.6 p. 1317-21
Publication Date: June 1992 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/92/$03.00
Language: English
Abstract: An n-channel **vertical** insulated-gate bipolar **transistor** (IGBT) process which implements a self-aligned p/sup +/ short inside the DMOS diffusion windows is proposed and demonstrated experimentally. The salient feature of the new process is the placement of a poly-Si plug to define the diffusion window of the p/sup +/ short. Similar forward conduction characteristics and tradeoffs with turn-off time were obtained for these self-aligned short IGBTs when compared to conventional IGBTs with non-self-aligned shorts. With a resistive load and no external gate resistor, dynamic latching current was seen to increase with increasing p/sup +/ diffusion depth and electron irradiation dosage, as well as with larger p/sup +/ diffusion windows.

Subfile: B

8/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

03157380 INSPEC Abstract Number: B88039480
Title: P-channel, **vertical** insulated gate bipolar **transistors** with collector short
Author(s): Chow, T.P.; Baliga, B.J.; Chang, H.R.; **Gray, P.V.**; Hennessy, W.; Logan, C.E.
Author Affiliation: Gen. Electr. Co., Schenectady, NY, USA
Conference Title: 1987 International Electron Devices Meeting, IEDM. Technical Digeset (Cat. No.87CH2515-5) p.670-3
Publisher: IEEE, New York, NY, USA
Publication Date: 1987 Country of Publication: USA 936 pp.
U.S. Copyright Clearance Center Code: CH2515-5/87/0000-0670$01.00
Conference Sponsor: IEEE
Conference Date: 6-9 Dec. 1987 Conference Location: Washington, DC, USA
Language: English
Abstract: P-channel, collector-shorted, **vertical** insulated gate bipolar **transistors** (IGBTs) with hexagonal and square cell geometries were studied. The presence of the collector short, surrounding the edges of the device, resulted in a linear I-V region before the conductivity modulation region sets in. The effect of poly-Si overlap and JFET (junction field-effect transistor) dosage on forward drop and breakdown voltage were analyzed for hexagonal and square DMOS cell geometries. In contrast to the conventional IGBT, the turnoff time increases with increasing collector current. A maximum controllable current of 5 A (710 A/cm/sup 2/) was measured when switching into 300 V at room temperature. The built-in antiparallel diode formed between the collector short and the deep n/sup +/ short in the DMOS cells has also been characterized.
Subfile: B

8/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01941250
E.I. Monthly No: EI8602017150
E.I. Yearly No: EI86122816
Title: INSULATED GATE TRANSISTOR: A NEW THREE-TERMINAL MOS-CONTROLLED BIPOLAR POWER DEVICE.
Author: Baliga, Jayant; Adler, Michael S.; Love, Robert P.; **Gray Peter V.**; Zommer, Nathan D.
Corporate Source: GE, High Voltage Device & Integrated Circuits Unit, Schenectady, NY, USA
Source: IEEE Transactions on Electron Devices v ED-31 n 6 Jun 1984 p 821-828
Publication Year: 1984
CODEN: IETDAI ISSN: 0018-9383
Language: ENGLISH
Abstract: A new three-terminal power device, called the insulated-gate transistor (IGT), with voltage-controlled output characteristics is described. In this device, the best features of the existing families of bipolar devices and power MOSFET's are combined to achieve optimal device characteristics for low-frequency power-control applications. Devices with

600-V blocking capability fabricated using a vertical DMOS process exhibit 20 times the conduction current density of an equivalent power MOSFET and five times that of an equivalent bipolar transistor operating at a current gain of 10. Typical gate turn-off times have been measured to range form 10 to 50 MU s. (Author abstract) 8 refs.

12/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013474613
WPI Acc No: 2000-646556/200062
Related WPI Acc No: 2003-695631
XRAM Acc No: C00-195491
XRPX Acc No: N00-479143

Contacting a silicide-based Schottky diode involves forming a silicide layer of Schottky diode, and contacting a contact to the silicide layer

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: DUNN J S; **GRAY P B**; KIEFT K K; SCHMIDT N T; ST ONGE S

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6121122	A	20000919	US 99312945	A	19990517	200062 B

Priority Applications (No Type Date): US 99312945 A 19990517
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6121122	A		8	H01L-029/64	

Abstract (Basic): US 6121122 A
Abstract (Basic):

NOVELTY - A silicide-based Schottky diode is contacted by forming a silicide layer of Schottky diode, where a first portion of the silicide layer is in contact with a guard ring area and a second portion of the silicide layer is not in contact with a guard ring area; and contacting a contact to the first portion of the silicide layer but not to the second portion.

USE - The method is used for contacting a silicide-based Schottky diode. The processes and structure of the invention may be used in any bi-complementary metal oxide semiconductor (**BiCMOS**), Bipolar, CMOS or other semiconductor technologies where diffusions are silicided.

ADVANTAGE - Schottky diode (20) is effectively de-coupled from contact metallurgy. In addition, the silicide/**silicon** interface is formed by a high temperature annealing process and is atomically clean and thermally stable. As contact metallurgy need only touch silicide layer over guard ring area, diode characteristics are not influenced by processes used to form contacts. Any etch or pre-clean steps may be used when defining contact and/or any typical thermal anneals may be used to ensure good ohmic contact to the silicide without influencing diode interface or its electrical characteristics.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a **silicon**-based Schottky diode.

Schottky diode (20)
Contact (36, 40, 42)
Silicide layer (46, 47)
Guard ring area (50)
Portion (54, 58)
External edge (60)
pp; 8 DwgNo 2/5

14/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015583356
WPI Acc No: 2003-645513/200361
Related WPI Acc No: 2003-446767
XRAM Acc No: C03-176407
XRPX Acc No: N03-513577

Quasi hyper-abrupt base-collector junction varactor for, e.g. mobile or cellular phones, includes antimony spike located between intrinsic base and subcollector region

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: COOLBAUGH D D; DUNN J S; GORDON M D; HAMMAD M Y; **JOHNSON J B**; SHERIDAN D C

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030122128	A1	20030703	US 200116539	A	20011213	200361 B
			US 2002323022	A	20021218	

Priority Applications (No Type Date): US 200116539 A 20011213; US 2002323022 A 20021218
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030122128	A1		10	H01L-029/04	Div ex application US 200116539 Div ex patent US 6521506

Abstract (Basic): US 20030122128 A1
Abstract (Basic):

NOVELTY - A quasi hyper-abrupt base-collector junction varactor comprises an antimony spike located between an intrinsic base and subcollector region of a bipolar device.

DETAILED DESCRIPTION - A quasi hyper-abrupt base-collector junction varactor comprises a substrate (10) having a collector region (18) of a first conductivity type atop a subcollector region (12), reach-through implant regions (20) located between at least a pair of isolation regions (16) of the collector region, a **silicon-germanium** layer atop a portion of the substrate not containing a reach-through implant region, and an antimony implant region located between an **extrinsic base** region and subcollector region. The **silicon-germanium** layer has the **extrinsic base** region of a second conductivity type that is different from the first conductivity type.

An INDEPENDENT CLAIM is also included for a method of fabricating the inventive quasi hyper-abrupt base-collector junction varactor.

USE - For mobile or cellular phones, personnel digital assistances, and other high radio frequency electronic devices.

ADVANTAGE - The assembly is highly linear, has improved tunability, can be easily implemented in existing complementary metal oxide semiconductor (CMOS) and **BiCMOS** technologies, and has the highest possible quality factor.

DESCRIPTION OF DRAWING(S) - The figure shows pictorial representation of the fabrication of a quasi hyper-abrupt base-collector junction varactor.

Substrate (10)
Subcollector region (12)
Isolation regions (16)
Collector region (18)
Reach-through implant regions (20)

17/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7239002 INSPEC Abstract Number: B2002-05-2570K-004
Title: A technology simulation methodology for AC-performance optimization of **SiGe** HBTs
Author(s): **Johnson, J.B.**; Stricker, A.; Joseph, A.J.; Slinkman, J.A.
Author Affiliation: Microelectron. Div., IBM, Essex Junction, VT, USA
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224) p.21.4.1-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 951 pp.
ISBN: 0 7803 7050 3 Material Identity Number: XX-2002-00101
U.S. Copyright Clearance Center Code: 0-7803-7050-3/01/$10.00
Conference Title: International Electron Devices Meeting. Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 2-5 Dec. 2001 Conference Location: Washington, DC, USA
Language: English
Abstract: A methodology for simultaneous calibration of **SiGe** HBT process and device simulation is presented and applied to **SiGe BiCMOS** HBTs with peak **cut-off frequencies** ranging from 100 GHz to 200 GHz. Predictive simulation capability is demonstrated for critical HBT AC device characteristics through comparison with experimental devices.
Subfile: B

performance and applications. The bandgap-engineered **SiGe** heterojunction bipolar transistors (HBTs) continue to be the workhorse of the technology, while the CMOS offering is fully foundry compatible for maximizing IP sharing. Process customization is done to provide high-quality passives, which greatly enables fully integrated single-chip solutions. Product examples include 40-Gb/s (OC768) components using high-speed **SiGe** HBTs, power amplifiers compatible for cellular applications, integrated voltage-controlled oscillators, and very high-level mixed-signal integration. It is argued that such key enablements along with the lower cost and higher yields attainable by **SiGe BiCMOS** technologies will provide competitive solutions for the communication marketplace.

Subfile: B

19/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

7554316 INSPEC Abstract Number: B2003-04-2570K-002

Title: Product applications and technology directions with **SiGe BiCMOS**

Author(s): Dunn, J.; Freeman, G.; Harame, D.; Joseph, A.; Coolbaugh, D.; Groves, R.; Stein, K.; Volant, R.; Subbanna, S.; Marangos, V.S.; St Onge, S.; Eshun, E.; Cooper, P.; **Johnson, J.**; Rieh, J.; Ramachandran, V.; Ahlgren, D.; Wang, D.; Wang, X.

Author Affiliation: IBM Corp., Essex Junction, VT, USA

Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrate Circuit Symposium. 24th Annual Technical Digest 2002 (Cat. No.02CH37354) p.135-8

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 2002 Country of Publication: USA x+296 pp.

ISBN: 0 7803 7447 9 Material Identity Number: XX-2002-02491

U.S. Copyright Clearance Center Code: 0-7803-7447-9/02/$17.00

Conference Title: IEEE Gallium Arsenide Integrated Circuits Symposium

Conference Sponsor: IEEE Electron Devices Soc.; IEEE Microwave Theory & Techniques Soc.; IEEE Solid-State Circuits Soc

Conference Date: 20-23 Oct. 2002 Conference Location: Monterey, CA, USA

Language: English

Abstract: In this paper we highlight the effectiveness and flexibility of **SiGe BiCMOS** as a technology platform over a wide range of performance and applications. Examples include high speed device design, power amplifiers, integrated VCOs and very high level integration.

Subfile: B

19/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

7509032 INSPEC Abstract Number: B2003-02-2570K-008

Title: High performance, low complexity 0.18 mu m **SiGe BiCMOS** technology for wireless circuit applications

Author(s): Feilchenfeld, N.; Lanzerotti, L.; Sheridan, D.; Wuthrich, R.; Geiss, P.; Coolbaugh, D.; **Gray, P.**; He, J.; Demag, P.; Greco, J.; Larsen, T.; Patel, V.; Zierak, M.; Hodge, W.; Rascoe, J.; Trappasso, J.; Orner, B.; Norris, A.; Hershberger, D.; Voegeli, B.; Voldman, S.; Rassel,

R.; Ramachandrian, V.; Gautsch, M.; Eshun, E.; Hussain, R.; Jordan, D.; St Onge, S.; Dunn, J.
Author Affiliation: IBM Microeletronics Div., Essex Junction, VT, USA
Conference Title: Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No.02CH37384) p.197-200
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA 241 pp.
ISBN: 0 7803 7561 0 Material Identity Number: XX-2002-02195
U.S. Copyright Clearance Center Code: 0-7803-7561-0/02/$17.00
Conference Title: 2002 IEEE Bipolar/BICMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Solid-State Circuits Soc
Conference Date: 29 Sept.-1 Oct. 2002 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: High frequency performance at low current density and low wafer cost is essential for low power wireless **BiCMOS** technologies. We have developed a low-complexity, ASIC-compatible, 0.18 mu m **SiGe BiCMOS** technology for wireless applications that offers 3 different breakdown voltage NPNs; with the high performance device achieving F/sub t//F/sub max/ of 60/85 GHz with a 3.0 V BV/sub CEO/. In addition, a full suite of high performance passive devices complement the state-of-the-art **SiGe** wireless HBTs.
Subfile: B

19/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6894354 INSPEC Abstract Number: B2001-05-2570K-002
Title: Review of **silicon-germanium BICMOS** technology after 4 years of production and future directions
Author(s): Subbana, S.; Freeman, G.; Ahlgren, D.; Jagannathan, B.; Greenberg, D.; **Johnson, J.**; Bacon, P.; Najarian, R.; Herman, D.; Meyeron, B.
Author Affiliation: Commun. Res. & Dev. Center, IBM Corp., Hopewell Junction, NY, USA
Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuits Symposium. 22nd Annual Technical Digest 2000. (Cat. No.00CH37084) p.7-10
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA ix+266 pp.
ISBN: 0 7803 5968 2 Material Identity Number: XX-2001-00190
U.S. Copyright Clearance Center Code: 0 7803 5968 2/2000/$10.00
Conference Title: GaAs IC Symposium. IEEE Gallium Arsenide Integrated Circuit Symposium. 22nd Annual Technical Digest 2000
Conference Sponsor: IEEE Electron Devices Soc.; IEEE Microwave Theory & Tech. Soc.; IEEE Solid-State Circuits Soc
Conference Date: 5-8 Nov. 2000 Conference Location: Seattle, WA, USA
Language: English
Abstract: **Silicon Germanium** (**SiGe**) HBTs have proven themselves as cheaper, viable replacements for GaAs in many different applications. **SiGe** RFIC products have been available for the last couple of years. **SiGe** SONET parts have also become available and demonstrate good performance. Adding to this product success, it has been possible to replace several GaAs chips with one **silicon-germanium** chip for yield, reliability, power, and cost improvements.

Integration with low-power, digital CMOS has also been demonstrated in different applications. Digital CMOS application-specific integrated circuits (ASICs) have been combined with **SiGe** HBT circuits. Various **SiGe BICMOS** ICs are in volume production in our CMOS fab. The quality of passive components such as inductors and capacitors is also approaching that of GaAs, enabling high-performance RF and networking circuits.
Subfile: B

19/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

6671304 INSPEC Abstract Number: B2000-09-1350H-056
Title: Prospects of **silicon-germanium**-based technology for very high-speed circuits
Author(s): Subbanna, S.; **Johnson**, J.; Freeman, G.; Volant, R.; Groves, R.; Herman, D.; Meyerson, B.
Author Affiliation: Microelectron., IBM Corp., Hopewell Junction, NY, USA
Conference Title: 2000 IEEE MTT-S International Microwave Symposium Digest (Cat. No.00CH37017) Part vol.1 p.361-4 vol.1
Editor(s): Perkins, T.
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 3 vol. lxviii+xxi+1976 pp.
ISBN: 0 7803 5687 X Material Identity Number: XX-2000-01754
U.S. Copyright Clearance Center Code: 0 7803 5687 X/2000/$10.00
Conference Title: 2000 IEEE MTT-S International Microwave Symposium Digest
Conference Date: 11-16 June 2000 Conference Location: Boston, MA, USA
Language: English
Abstract: **Silicon-germanium** (**SiGe**) heterojunction bipolar transistor (HBT) **BiCMOS** technology has developed into a production manufacturing technology that replaces and extends the performance of **silicon**-based **BiCMOS** technology. The market impetus for this development has been the insatiable requirement for bandwidth in network communication at speeds up to 40 Gbit/s and the rapid growth of the global cellular and wireless LAN markets. There has also been much work on the use of **silicon** -based structures for microwave frequencies. This paper focuses on a review of the status of our **SiGe** **BiCMOS** technology, based on four generations of scaling CMOS-compatible **SiGe** . We also show in principle how techniques commonly used in Ill-V semiconductor technology and microwave systems can also be applied to **SiGe** chips, along with **silicon**-on-insulator (SOI) and other existing technology, to provide a possible further extension in **SiGe** performance, for 50+ GHz circuits.
Subfile: B

19/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

6521143 INSPEC Abstract Number: B2000-04-2570K-003
Title: A 0.24 mu m **SiGe** **BiCMOS** mixed-signal RF production technology featuring a 47 GHz f/sub t/ HBT and 0.18 mu m L/sub ett/ CMOS
Author(s): St. Onge, S.A.; Harame, D.L.; Dunn, J.S.; Subbanna, S.;

Ahlgren, D.C.; Freeman, G.; Jagannathan, B.; Jeng, J.; Schonenberg, K.; Stein, K.; Groves, R.; Coolbaugh, D.; Feilchenfeld, N.; Geiss, P.; Gordon, M.; **Gray**, P.; Hershberger, D.; Kilpatrick, S.; Johnson, R.; Joseph, A.; Lanzerotti, L.; Malinowski, J.; Orner, B.; Zierak, M.

Author Affiliation: Microelectron. Div., IBM Corp., Essex Junction, VT, USA

Conference Title: Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No.99CH37024) p.117-20

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 182 pp.

ISBN: 0 7803 5712 4 Material Identity Number: XX-1999-02917

U.S. Copyright Clearance Center Code: 0 7803 5712 4/99/$10.00

Conference Title: Proceedings of the 1999 Bipolar/BiCMOS Circuits and Technology Meeting

Conference Sponsor: IEEE

Conference Date: 26-28 Sept. 1999 Conference Location: Minneapolis, MN, USA

Language: English

Abstract: A new base-after-gate integration scheme has been developed to integrate a 47 GHz f/sub t/, 65 GHz F/sub max/**SiGe** HBT process with a 0.24 mu m CMOS technology having 0.18 mu m L/sub eff/ and 5 nm gate oxide. We discuss the benefits and challenges of this integration scheme which decouples the HBT from the CMOS thermal cycles. We also describe the resulting 0.24 mu m **SiGe BiCMOS** technology, **BiCMOS** 6HP, which includes a 7 nm dual gate oxide option and full suite of passive components. The technology provides a high level of integration for mixed-signal RF applications.

Subfile: B

19/3,AB/8 (Item 8 from file: 2)

DIALOG(R)File 2:INSPEC

6507006 INSPEC Abstract Number: B2000-03-1350H-049

Title: A 0.18 mu m 90 GHz f/sub T/ **SiGe** HBT **BiCMOS**, ASIC-compatible, copper interconnect technology for RF and microwave applications

Author(s): Freeman, G.; Ahlgren, D.; Greenberg, D.R.; Groves, R.; Huang, F.; Hugo, G.; Jagannathan, B.; Jeng, S.J.; **Johnson**, **J.**; Schonenberg, K.; Stein, K.; Volant, R.; Subbanna, S.

Author Affiliation: IBM Corp., Hopewell Junction, NY, USA

Conference Title: International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318) p.569-72

Publisher: IEEE, Piscataway, NJ, USA

Publication Date: 1999 Country of Publication: USA 943 pp.

ISBN: 0 7803 5410 9 Material Identity Number: XX-2000-00353

U.S. Copyright Clearance Center Code: 0 7803 5410 9/99/$10.00

Conference Title: International Electron Devices Meeting 1999. Technical Digest

Conference Sponsor: Electron Devices Soc. IEEE

Conference Date: 5-8 Dec. 1999 Conference Location: Washington, DC, USA

Language: English

Abstract: We present a self-aligned, 0.18 mu m emitter width **SiGe** HBT with f/sub T/ of 90 GHz, f/sub MAX/ of 90 GHz (both at V/sub CB/=0.5 V), NF/sub MIN/ of 0.4 dB, and BV/sub CEO/ of 2.7 V. We also demonstrate that this device is integrable with IBM's 0.18 mu m, 1.8/3.3 V copper metallization CMOS technology with little effect on the CMOS device

cost is essential for low power wireless **BiCMOS** technologies. We have developed a low-complexity, ASIC compatible, 0.18 um **SiGe BiCMOS** technology for wireless applications that offers 3 different breakdown voltage NPNs with the high performance device achieving F//t/F//m//a//x of 60/85 GHz with a 3.0 V BV//C//E//O. In addition, a full suite of high performance passive devices complement the state-of-the-art **SiGe** wireless HBTs. 6 Refs.

19/3,AB/11 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05967245
E.I. No: EIP01536782825
Title: A 0.18mum **BiCMOS** technology featuring 120/100 GHz (f//t/f//m//a//x) HBT and ASIC-compatible CMOS using copper interconnect
Author: Joseph, A.; Coolbaugh, D.; Zierak, M.; Wuthrich, R.; Geiss, P.; He, Z.; Liu, X.; Orner, B.; **Johnson, J.**; Freeman, G.; Ahlgren, D.; Jagannathan, B.; Lanzerotti, L.; Ramachandran, V.; Malinowski, J.; et al.
Corporate Source: IBM Microelectronics Division, Essex Junction, VT 05452, United States
Conference Title: 2001 BIPOLAR/BICMOS CIRCUITS AND TECHNOLOGY MEETING
Conference Location: Minneapolis, MN, United States Conference Date: 20010930-20011002
E.I. Conference No.: 58877
Source: Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting 2001. p 143-146 (IEEE cat n 01CH37212)
Publication Year: 2001
CODEN: PBCMFL
Language: English
Abstract: A **BiCMOS** technology is presented that integrates a high performance NPN (f//T = 120GHz and f//m//a//x = 100GHz), ASIC compatible 0.11mum L//e//f//f CMOS, and a full suite of passive elements. Significant HBT performance enhancement compared to the previously published results in left bracket 1 right bracket has been achieved through further collector and base profile optimization guided by process and device simulations. Base transit time reduction was achieved by simultaneously increasing the **Ge** ramp and by limiting the base diffusion with the addition of carbon doping to **SiGe** epitaxial base. This paper describes IBM's next generation **SiGe BiCMOS** production technology targeted at the communications market. 6 Refs.

19/3,AB/12 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

04887060 INSIDE CONFERENCE ITEM ID: CN050968337
A 0.13mum **BiCMOS** Technology Featuring a 200/280GHz (f SUB T/f SUB m SUB a SUB x) **SiGe** HBT
Orner, B. A.; Liu, Q. Z.; Rainey, B.; Stricker, A.; Geiss, P.; **Gray**, P.; Zierak, M.; Gordon, M.; Collins, D.; Ramachandran, V.
CONFERENCE: Bipolar/BiCMOS circuits and technology meeting
PROCEEDINGS OF THE BIPOLAR BICMOS CIRCUITS AND TECHNOLOGY MEETING , 2003
P: 203-206
IEEE, 2003
ISSN: 1088-9299
LANGUAGE: English DOCUMENT TYPE: Conference Preprinted papers and programme

26feb04 10:10:20 User267149 Session D1260.1

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File 347:JAPIO Oct 1976-2003/Oct(Updated 040202)
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*File 347: JAPIO data problems with year 2000 records are now fixed. Alerts have been run. See HELP NEWS 347 for details.
File 344:Chinese Patents Abs Aug 1985-2003/Nov
(c) 2003 European Patent Office
File 371:French Patents 1961-2002/BOPI 200209
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*File 371: This file is not currently updating. The last update is 200209.

Set	Items	Description
S1	5900	VERTICAL?(3N)(NPN OR PNP OR TRANSIST?)
S2	4344	PNP(3N)TRANSIST? AND NPN(3N)TRANSIST?
S3	14768	BICMOS OR BIPOLAR()COMPLEMENTARY()METAL()OXIDE
S4	12723	MC=(U13-D03B2 OR U11-C18A OR U13-D02A)
S5	436062	MOS OR METAL()OXIDE(1W)SEMICONDUCT??????? OR NMOS? ? OR N(-)MOS? ? OR PMOS? ? OR P()MOS? ? OR VMOS? ? OR V()MOS? ? OR C(-)MOS? ? OR CMOS? ? OR NMOSFET? ? OR NMOS()FET? ? OR PMOS()FET? ? OR PMOSFET? ?
S6	110956	DMOS()FET? ? OR DMOSFET? ? OR UMOS()FET? ? OR UMOSFET? ? OR MOS()FET? ? OR MOSFET? ?
S7	169626	(FIELD()EFFECT? ?(1W)TRANSIT???????) OR FET? ?
S8	653332	S1:S7
S9	610671	HIGH?????(3N)PERFORM???????
S10	512	PERFORM???????(3N)(NPN OR PNP)
S11	610948	S9:S10
S12	276981	(P OR N)(1N)(TYPE? ? OR EMIT??????)
S13	112717	(SILICON OR SI) AND (GERMANIUM OR GE)
S14	36120	SILICON()GERMANIUM OR SIGE
S15	122303	S13:S14
S16	69935	(N OR P)(1N)(BASE??? OR REGION? ?)
S17	45956	(BASE??? OR REGION? ?)(3N)(EXTRINSIC? OR EXTERNAL? OR OUTSIDE)
S18	124712	(INTRINSIC? OR INTERNAL? OR INNER? OR WITHIN OR INSIDE)(3N)REGION? ?
S19	233710	S16:S18
S20	63100	(CUTOFF OR CUT()OFF OR LIMIT??????)(3N)(FREQUENC? OR GHZ OR GIGAHERTZ)
S21	418903	RF OR RADIO(3N)FREQUENC????? OR RADIOFREQUENC??????
S22	4788	MASK??????(3N)STEP? ?
S23	21676	S8 AND S11
S24	1206	S23 AND S12
S25	73	S24 AND S15
S26	12	S25 AND S19
S27	6	RD (unique items)
S28	61	S25 NOT S26
S29	17	S28 AND S20
S30	9	RD (unique items)
S31	44	S28 NOT S29
S32	0	S31 AND S21
S33	0	S31 AND S22
S34	32	RD S31 (unique items)
S35	0	S34 AND S2
S36	1	S34 AND S1
S37	31	S34 NOT S36
S38	436	S1 AND S2
S39	39	S38 AND S3
S40	0	S39 AND S15
S41	10	S39 AND S19
S42	10	RD (unique items)
S43	10	S42 NOT S27,S30,S34
S44	957	S15 AND S20
S45	2	S44 AND S22
S46	1	RD (unique items)
S47	115	S44 AND S21
S48	6	S47 AND S19
S49	4	RD (unique items)

S50 4 S49 NOT S45

27/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7223279 INSPEC Abstract Number: B2002-05-2570K-001
Title: Minimizing thermal resistance and collector-to-substrate capacitance in **SiGe BiCMOS** on SOI
Author(s): Mastrapasqua, M.; Palestri, P.; Pacelli, A.; Celler, G.K.; Frei, M.R.; Smith, P.R.; Johnson, R.W.; Bizzarro, L.; Lin, W.; Ivanov, T.G.; Carroll, M.S.; Kizilyalli, I.C.; King, C.A.
Author Affiliation: Agere Syst., Murray Hill, NJ, USA
Journal: IEEE Electron Device Letters vol.23, no.3 p.145-7
Publisher: IEEE,
Publication Date: March 2002 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200203)23:3L.145:MTRC;1-2
Material Identity Number: I338-2002-004
U.S. Copyright Clearance Center Code: 0741-3106/02/$17.00
Language: English
Abstract: We describe a low fabrication cost, **high-performance** implementation of **SiGe BiCMOS** on SOL The use of high-energy implant allows the simultaneous formation of the subcollector and an additional **n-type region** below the buried oxide. The combination of buried oxide layer and floating **n-type region** underneath results in a very low collector-to-substrate capacitance. We also show that this process option achieves a much lower thermal resistance than using SOI with deep trench isolation, both reducing cost and curbing self-heating effects.
Subfile: B

27/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06447123
E.I. No: EIP03297544958
Title: 2D-simulation and analysis of lateral SiC **N-emitter** SiGe **P-base** Schottky metal-collector (NPM) HBT on SOI
Author: Kumar, M. Jagadesh; Reddy, C. Linga
Corporate Source: Department of Electrical Engineering Indian Inst. of Technology, Delhi, Hauz Khas, New Delhi 110 016, India
Source: Microelectronics Reliability v 43 n 7 July 2003. p.1145-1149
Publication Year: 2003
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: We report a novel **BiCMOS** compatible lateral SiC **N-emitter**, SiGe **P-base** Schottky metal-collector NPM HBT on SOI. The proposed lateral NPM HBT performance has been evaluated in detail using 2-dimensional device simulation by comparing it with the equivalent NPN HBT and homojunction silicon NPM BJT structures. Based on our simulation results, it is observed that while both the lateral NPM and NPN HBTs exhibit high current gain, high cut-off frequency compared to the homojunction NPN BJT, the lateral NPM HBT has the additional benefit of suppressed Kirk effect and excellent transient response over its counterpart lateral **NPN** HBT. The improved **performance** of the proposed NPM HBT is discussed in detail and a **CMOS** compatible process is suggested for its fabrication. copy 2003 Elsevier Ltd. All

rights reserved. 26 Refs.

27/3,AB/3 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci
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01813033 Genuine Article#: JC979 Number of References: 32
Title: COMPARATIVE-ANALYSIS OF THE **HIGH**-FREQUENCY **PERFORMANCE** OF SI/SI1-XGEX HETEROJUNCTION BIPOLAR AND SI BIPOLAR-TRANSISTORS (Abstract Available)
Author(s): CHEN J; GAO GB; MORKOC H
Corporate Source: INTEL CORP,PORTLAND TECHNOL DEV,AL4-76,5200 NE ELAM YOUNG PKWY/HILLSBORO//OR/97124; UNIV ILLINOIS,COORDINATED SCI LAB/URBANA//IL/61801; UNIV ILLINOIS,MAT RES LAB/URBANA//IL/61801
Journal: SOLID-STATE ELECTRONICS, 1992, V35, N8 (AUG), P1037-1044
Language: ENGLISH Document Type: ARTICLE
Abstract: This paper presents a model-based comparison of the **high**-frequency **performance** of Si/Si1-xGex heterojunction bipolar transistors (HBTs) and Si bipolarjunction transistors (BJTs), in which the structural parameters were designed for maximum f(T) almost-equal-to f(max). This model study shows: (1) the Si1-xGex HBT has a peak f(T)(=f(max)) of 64 GHz, which represents a 16.4% improvement over the Si BJT; (2) emitter charging time has a sizable effect on **high**-frequency **performance**, even at current densities as high as 80 kA cm-2; (3) compositional grading of the **SiGe** base, as well as the profile of the base doping, strongly influence f(T) and f(max). A Gaussian grading profile is found to exhibit the highest peak f(T)=f(max); a 30% higher peak cutoff frequency is predicted over a uniform doping profile; (4) the dependence of **high**-frequency **performance** upon collector design represents a trade-off between f(T), f(max) and BV(CBO); and (5) by decreasing emitter or base doping levels, Si1-xGexHBTs with f(T) exceeding 100 GHz can be designed. Alternatively, f(max) of 100 GHz may be achieved by increasing **base** doping and reducing **extrinsic** capacitances and resistances.

27/3,AB/4 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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015608851
WPI Acc No: 2003-671008/200363
XRAM Acc No: C03-182928
XRPX Acc No: N03-535814
Integrated circuit fabricated in semiconductor material of first conductivity type, comprises source and drain, well of opposite conductivity, semiconductor region, and layer of opposite conductivity type
Patent Assignee: SALLING C T (SALL-I); WU Z (WUZZ-I); TEXAS INSTR INC (TEXI)
Inventor: SALLING C T; WU Z
Number of Countries: 102 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030134479	A1	20030717	US 200251962	A	20020116	200363	B
WO 200363235	A1	20030731	WO 2003US1412	A	20030116	200363	

Priority Applications (No Type Date): US 200251962 A 20020116

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030134479 A1			13	H01L-021/336	
WO 200363235	A1	E		H01L-021/8238	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SC SD SE SG SK SL TJ TM TN TR TT TZ UA UG US UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT SD SE SI SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20030134479 A1

Abstract (Basic):

NOVELTY - An integrated circuit fabricated in semiconductor material of first conductivity type, the circuit having surface(s) of lateral **metal oxide semiconductor** (**MOS**) transistor surrounded by electrical isolation region, has source and drain, well of opposite conductivity type surrounding the source and drain, semiconductor **region within** the semiconductor material, and layer of opposite conductivity type.

DETAILED DESCRIPTION - The integrated circuit comprises source and drain, each having at the surface region of the opposite conductivity type extending to centrally located gate, defining the active area of the transistor; well of the opposite conductivity type surrounding the source and drain, extending from the surface deep into the semiconductor material; semiconductor **region within** the semiconductor material surrounded by the well and having a resistivity higher than a remainder of the semiconductor material; and layer of the opposite conductivity type buried in the semiconductor region. The layer extends laterally to the well, thus electrically isolating a near-surface portion of the semiconductor region from the remainder of the semiconductor material, and enabling the **MOS** transistor to operate as an electrically isolated high-voltage input/output (I/O) transistor for circuit noise reduction, while having low drain junction capacitance. This layer extends vertically deeper from the surface than the electrical isolation region, thus enabling a separate contact to the electrically isolated near-surface portion of the semiconductor region. INDEPENDENT CLAIMS are also included for:

(1) a method of fabricating an electrically isolated high-voltage I/O **nMOS** transistor in the surface of a **p-type** semiconductor material, comprising forming 2 nested pairs of non-conductive electrical isolation regions into the **p-type** semiconductor material, the inner pair defining lateral boundaries of the transistor active area, and the outer pair defining areas between n-wells; implanting p-doping or n-doping ions to adjust background doping level of sub-surface region of the **p-type** material; forming n-wells into the adjusted **p-type** material; depositing over the surface a layer of insulating material as gate dielectric, covering the transistor area; depositing a layer of **polysilicon** or other conductive material onto the insulating layer; protecting a portion of the **polysilicon** and etching its remainder, defining gate area of the transistor; depositing first photoresist layer and opening a window in there, exposing the surface of the area between outer isolation regions; implanting, at low energy, n-doping ions into the exposed surface area, creating shallow n-doped layers under the surface as extended source and drain of the transistor; implanting, at high energy and high dose, n-doping ions into the exposed surface area, creating a deep region under the surface

having net **n-type** doping between, and continuous with, the n-wells, and further creating **p-region** having doping concentration lower than that of the remainder of the adjusted **p-type region**; removing the first photoresist layer; depositing conformal insulating layer of an insulator, such as **silicon** nitride or **silicon** dioxide, over the surface and directional plasma etching the insulating layers so that only sidewalls around the **polysilicon** remain; depositing second photoresist layer and opening a window in there, exposing the surface of the area between the outer isolation regions; implanting, at medium energy, n-doping ions in the exposed surface area, creating **n**-doped **region** that extends to a medium depth under the surface as deep source and drain of the transistor; removing the second photoresist layer; and forming an electrical contact region to the **p-region** of lower doping concentration;

(2) a method of fabricating a buried **p-type** layer connecting 2 p-wells in an **n-type** semiconductor region, electrically isolating the near-surface **n-type** semiconductor portion for fabricating a high-voltage I/O **pMOS** transistor, comprising depositing a photoresist layer over the surface of the **n-type region** and opening a window in the layer, exposing the surface area between the p-wells; implanting, at low energy, p-doping ions through the window, creating shallow p-doped layers under the surface as extended source and drain of the transistor; and implanting, at high energy and high dose, p-doping ions into the **n-type** semiconductor through the window, creating a deep region having net **p-type** doping between; and

(3) a method of fabricating an electrically isolated high-voltage I/O **pMOS** transistor in the surface of **n-type** semiconductor material.

USE - Used as integrated circuit applicable to **nMOS** and **pMOS** transistors (claimed).

ADVANTAGE - The assembly provides transistors operable to eliminate substrate noise.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross-section of electrically isolated high-voltage I/O **nMOS** transistor.

Substrate (101)
Isolation trench (102)
Gate (103)
Gate insulator (104)
Deep source (110)
Extended source (111)
Deep drain (112)
Photoresist layer (130)
High energy ion implant (140)
Buried layer (160)
pp; 13 DwgNo 1/7

27/3,AB/5 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015302307
WPI Acc No: 2003-363241/200334
XRAM Acc No: C03-095975
XRPX Acc No: N03-290079

Circuit for processing radio frequency signal comprises field effect transistor(s) having channel region including strained channel layer(s) disposed on planarized layer(s)

Patent Assignee: BRAITHWAITE G (BRAI-I); CURRIE M (CURR-I); HAMMOND R (HAMM-I); AMBERWAVE SYSTEMS CORP (AMBE-N)
Inventor: BRAITHWAITE G; CURRIE M; HAMMOND R
Number of Countries: 101 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 200328106	A2	20030403	WO 2002US30226	A	20020924	200334	B
US 20030102498	A1	20030605	US 2001324329	P	20010924	200339	
			US 2002253361	A	20020924		

Priority Applications (No Type Date): US 2001324329 P 20010924; US 2002253361 A 20020924
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 200328106	A2	E	26	H01L-027/088	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NO NZ OM PH PL PT RO RU SD SE SG SI SK SL TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW
Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU MC MW MZ NL OA PT SD SE SK SL SZ TR TZ UG ZM ZW

US 20030102498	A1		H01L-029/76	Provisional application US 2001324329

Abstract (Basic): WO 200328106 A2
Abstract (Basic):

NOVELTY - A circuit for processing a radio frequency (RF) signal comprises field effect transistor(s) (**FET**(s)) (100) to which the RF signal is applied. The **FET**(s) comprises a semiconductor substrate (102) including a planarized layer(s), a channel region (110) including a strained channel layer(s) disposed on the planarized layer(s) and a gate electrode (116).

USE - Processing RF signal (claimed).

ADVANTAGE - Provides RF signals that exhibit improved **performance**, particularly at **high** signal frequencies without requiring significant changes to design or fabrication.

DESCRIPTION OF DRAWING(S) - The figure is a cross-section of the field effect transistor.

Field effect transistor (100)
Semiconductor substrate (102)
Isolation well (104)
Isolation trenches (106)
Channel region (110)
Gate electrode (116)
pp; 26 DwgNo 1/6

27/3,AB/6 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

05230749
SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.: 08-186249 [JP 8186249 A]
PUBLISHED: July 16, 1996 (19960716)
INVENTOR(s): AWANO YUJI
MAEDA TAKESHI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 06-327156 [JP 94327156]
FILED: December 28, 1994 (19941228)

ABSTRACT

PURPOSE: To obtain a **high-performance** complementary semiconductor circuit device having a higher-speed characteristic than a **silicon** complementary circuit device, by simple manufacturing processes and with good reproducibility.

CONSTITUTION: A grated **Si**(sub 1-x)**Ge**(sub x) layer 2 having an increasing **Ge** composition, an active layer 3 composed mainly of **germanium**, and a grated **Si**(sub 1-y)**Ge**(sub y) layer 4 having a reducing **Ge** composition are provided on a **silicon germanium** substrate 1, and in its one part **region** a **p-type** transistor 7 having a **silicon germanium** active layer 3 as a channel layer is formed. Along with it, in an adjacent **region** an **n-type** transistor 8 is formed in a III-V compound semiconductor active layer 6 provided through the medium of a high-resistance III-V compound semiconductor layer 5.

30/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7511920 INSPEC Abstract Number: B2003-03-1350F-003
Title: DC and **high** frequency **performance** of 0.1 mu m **n-type** **Si**/**Si**/sub 0.6/**Ge** /sub 0.4/ MODFET with f/sub MAX/=188 GHz at 300 K and f/sub MAX/=230 GHz at 50 K
Author(s): Enciso-Aguilar, M.; Aniel, F.; Crozat, P.; Adde, R.; Herzog, H.-J.; Hackbarth, I.; Konig, U.; von Kanel, H.
Author Affiliation: Inst. d'Electron. Fondamentale, Univ. de Paris-Sud, Orsay, France
Journal: Electronics Letters vol.39, no.1 p.149-51
Publisher: IEE,
Publication Date: 9 Jan. 2003 Country of Publication: UK
CODEN: ELLEAK ISSN: 0013-5194
SICI: 0013-5194(20030109)39:1L.149:HFPT;1-1
Material Identity Number: E089-2003-001
U.S. Copyright Clearance Center Code: 0013-5194/03/$20.00
Language: English
Abstract: Maximum oscillation frequency f/sub MAX/ as high as 188 GHz at 300 K and 227 GHz at 50 K are reported for a 0.1*30 mu m/sup 2/ **n-type** strained **Si**/**Si**/sub 0.6/**Ge**/sub 0.4/ modulation doped field-effect transistor (n-MODFET) together with high quality DC characteristics. These f/sub MAX/ are the highest values reported so far for **Si**-based hetero-**FETs** . The frequency performances are discussed using analytical expressions of f/sub MAX/ and f/sub Ti/ (intrinsic current gain **cutoff** **frequency**) together with the main equivalent circuit elements extracted.
Subfile: B

30/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6851873 INSPEC Abstract Number: B2001-04-2560S-012
Title: **SiGe**-based **FETs**: buffer issues and device results
Author(s): Herzog, H.-J.; Hackbarth, T.; Hock, G.; Zeuner, M.; Konig, U.
Author Affiliation: Res. Center, Daimler-Chrysler AG, Ulm, Germany
Journal: Thin Solid Films Conference Title: Thin Solid Films (Switzerland) vol.380, no.1-2 p.36-41
Publisher: Elsevier,
Publication Date: 22 Dec. 2000 Country of Publication: Switzerland
CODEN: THSFAP ISSN: 0040-6090
SICI: 0040-6090(20001222)380:1/2L.36:SBFB;1-R
Material Identity Number: T070-2001-003
U.S. Copyright Clearance Center Code: 0040-6090/2000/$20.00
Conference Title: 2000 E-MRS Spring Conference, Symposium F: Thin Films Epitaxial Growth and Nanostructures
Conference Date: 29 May-2 June 2000 Conference Location: Strasbourg, France
Language: English
Abstract: **SiGe** quantum well structures gain increasing interest in the **Si** technology. The preparation of a **Si** channel or a **Ge**-rich or even a pure **Ge** channel with a respective two-dimensional carrier gas opens the attractive possibility to fabricate **high** **performance** n- or **p-type** field effect

transistors. For both device types, a virtual substrate surface is required which is created by a strain relieved buffer layer grown on a **Si** standard wafer. The paper reviews various approaches of **SiGe** buffers including special attempts to reduce the thickness and to improve the quality. N- and **p-type** modulation-doped field-effect transistors are presented which show comparably good device characteristics and **cut-off frequencies** in the range of 100-120 GHz.
Subfile: B

30/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

6674315 INSPEC Abstract Number: B2000-09-1350F-027
Title: **High performance** 0.1 mu m gate-length **p-type SiGe** MODFET's and **MOS**-MODFET's
Author(s): Lu, W.; Kuliev, A.; Koester, S.J.; Wang, X.-W.; Chu, J.O.; Ma, T.-P.; Adesida, I.
Author Affiliation: Microelectron. Lab., Illinois Univ., Urbana, IL, USA
Journal: IEEE Transactions on Electron Devices vol.47, no.8 p. 1645-52
Publisher: IEEE,
Publication Date: Aug. 2000 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
SICI: 0018-9383(200008)47:8L.1645:HPGL;1-0
Material Identity Number: I037-2000-008
U.S. Copyright Clearance Center Code: 0018-9383/2000/$10.00
Language: English
Abstract: **High performance p-type** modulation-doped field-effect transistors (MODFET's) and **metal-oxide-semiconductor** MODFET (**MOS** -MODFET) with 0.1 mu m gate-length have been fabricated on a high hole mobility **SiGe-Si** heterojunction grown by ultrahigh vacuum chemical vapor deposition. The MODFET devices exhibited an extrinsic transconductance (g/sub m/) of 142 mS/mm, a unity current gain **cut-off frequency** (f/sub T/) of 45 GHz and a maximum oscillation frequency (f/sub MAX/) of 81 GHz, 5 nm-thick high quality jet-vapor-deposited (JVD) SiO/sub 2/ was utilized as gate dielectric for the **MOS**-MODFET's. The devices exhibited a lower gate leakage current (1 nA/ mu m at V/sub gs/=6 V) and a wider gate operating voltage swing in comparison to the MODFET's. However, due to the larger gate-to-channel distance and the existence of a parasitic surface channel, **MOS** -MODFET's demonstrated a smaller peak g/sub m/ of 90 mS/mm, f/sub T/ of 38 GHz, and f/sub max/ of 64 GHz. The threshold voltage shifted from 0.45 V for MODFET's to 1.33 V for **MOS**-MODFET's. A minimum noise figure (NF/sub min/) of 1.29 dB and an associated power gain (G/sub a/) of 12.8 dB were measured at 2 GHz for MODFET's, while the **MOS** -MODFET's exhibited a NF/sub min/ of 0.92 dB and a G/sub a/ of 12 dB at 2 GHz. These DC, RF, and high frequency noise characteristics make **SiGe/Si** MODFET's and **MOS**-MODFET's excellent candidates for wireless communications.
Subfile: B

30/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6507008 INSPEC Abstract Number: B2000-03-2560R-134
Title: **High performance** 0.15 mu m self-aligned **SiGe p-MOS**-MODFET's with SiN gate dielectric
Author(s): Lu, W.; Hammond, R.; Koester, S.J.; Wang, X.W.; Chu, J.O.; Ma, T.P.; Adesida, I.
Author Affiliation: Dept. of Electr. & Comput. Eng., Illinois Univ., Urbana, IL, USA
Conference Title: International Electron Devices Meeting 1999. Technical Digest (Cat. No.99CH36318) p.577-80
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1999 Country of Publication: USA 943 pp.
ISBN: 0 7803 5410 9 Material Identity Number: XX-2000-00353
U.S. Copyright Clearance Center Code: 0 7803 5410 9/99/$10.00
Conference Title: International Electron Devices Meeting 1999. Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 5-8 Dec. 1999 Conference Location: Washington, DC, USA
Language: English
Abstract: Using jet-vapor-deposited **silicon** nitride as gate dielectric, self-aligned **p-type SiGe metal-oxide-semiconductor** modulated-doped field effect transistors are fabricated. For a 0.15 mu m gate-length device, the gate leakage current is as low as 0.46 nA/ mu m at V/sub gs/=3 V and V/sub ds/=-50 mV. A maximum extrinsic transconductance of 305 mS/mm, a unity current gain **cut-off frequency** of 62 **GHz** , and a maximum oscillation frequency of 68 GHz are measured at low operating biases of V/sub ds/=-0.75 V and V/sub gs/=0.4 V.
Subfile: B

30/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5285918 INSPEC Abstract Number: B9607-2560S-024
Title: **High performance** submicron-gate **SiGe p-type** modulation-doped field-effect transistors
Author(s): Arafa, M.; Fay, P.; Ismail, K.; Chu, J.O.; Meyerson, B.S.; Adesida, I.
Author Affiliation: Coordinated Sci. Lab., Illinois Univ., Urbana, IL, USA
Conference Title: 1995 53rd Annual Device Research Conference Digest (Cat. No.95TH8109) p.20-1
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 170 pp.
ISBN: 0 7803 2788 8 Material Identity Number: XX96-00544
Conference Title: 1995 53rd Annual Device Research Conference Digest
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 19-21 June 1995 Conference Location: Charlottesville, VA, USA
Language: English
Abstract: High transconductance **p-type** field-effect transistors (**FETs**) are essential for the fabrication of high speed complementary circuits. Unfortunately, the much lower mobility of holes in comparison to electrons in **Si** has been responsible for the large gap between the performance of **n-type** and **p-type** devices. Recent advances in the growth of high quality **SiGe** has lead to structures with higher hole mobilities. This has been attributed to the

light hole-heavy hole band splitting which results in less band mixing and a smaller in-plane effective mass. In this work, we report our work on the fabrication and characterization of **p-type** modulation-doped field effect transistors (MODFETs) in high mobility **SiGe** heterostructures. High transconductance and unity current-gain **cut-off frequency** are demonstrated for submicron-gate MODFETs.
Subfile: B

30/3,AB/6 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05135815
E.I. No: EIP98104417498
Title: **High performance** 0.25 mu m **p-type Ge** /**SiGe** MODFETs
Author: Hoeck, G.; Hackbarth, T.; Erben, U.; Kohn, E.; Koenig, U.
Corporate Source: Univ of Ulm, Ulm, Ger
Source: Electronics Letters v 34 n 19 Sep 17 1998. p 1888-1889
Publication Year: 1998
CODEN: ELLEAK ISSN: 0013-5194
Language: English
Abstract: The authors report the fabrication and characterization of 0.25 mu m gate length **p-type Ge** channel modulation doped field effect transistors (MODFETs) with improved RF performance. The structure consists of a compressively strained pure **Ge** hole channel, grown on a relaxed 5 mu m thick graded **Si**//0//.//4Ge//0//.//6 buffer. A room temperature hole mobility of 1870 cm**2/Vs and a sheet carrier density of 2.1 multiplied by 10**1**2cm** minus **2 were measured. The devices exhibit DC transconductances up to 160 mS/mm and saturation currents up to 300 mA/mm. **Cutoff frequencies** of f//T equals 32 GHz and f//m//a//x equals 85 GHz have been achieved. (Author abstract) 6 Refs.

30/3,AB/7 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03053266
E.I. Monthly No: EIM9104-017183
Title: **SiGe**-base **PNP transistors** fabricated with **n-type** UHV/CVD LTE in a 'No Dt' process.
Author: Harame, D. L.; Stork, J. M. C.; Meyerson, B. S.; Crabbe, E. F.; Patton, G. L.; Scilla, G. J.; de Fresart, E.; Bright, A. A.; Stanis, C.; Megdanis, A. C.; Manny, M. P.; Petrillo, E. J.; Dimeo, M.; McIntosh, R. C.; Chan, K. K.
Corporate Source: IBM T J Watson Res Center, Yorktown Heights, NY, USA
Conference Title: 1990 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19900604
E.I. Conference No.: 14179
Source: Digest of Technical Papers Digest of Technical Papers - Symposium on VLSI Technology. Publ by IEEE, IEEE Service Center, Piscataway, NJ, USA (IEEE cat n 90CH2874-6). p 47-48
Publication Year: 1990
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: Experimental results are presented on the use of **N-type** ultrahigh-vacuum/chemical vapor deposition (UHV/CVD)

low-temperature epitaxy (LTE) to deposit thin (45 nm), heavily doped (1 multiplied by 10**1**9 cm**-**3) **SiGe** films to form the base of **PNP transistors**. To take full advantage of epitaxial base technology, the thermal cycles following the base deposition that cause dopant diffusion and relaxation of highly strained layers, must be eliminated. This objective is met by a novel process using PECVD insulators and UHV/CVD LTE emitter deposition to limit the temperature following the base deposition to 550 degree C. This is essentially a 'No Dt' process in the sense that the effective dopant diffusion length Dt is negligible at this temperature. An advanced double-polysilicon bipolar structure was modified to fabricate non-self-aligned small-geometry transistors. Both DC and AC measurements were used to characterize the devices, confirming the presence of a large valence band offset at the base-collector junction. The resulting barrier to minority carrier transport caused additional charge storage in the neutral base and **limited** the peak **cutoff frequency** to 15 **GHz** independent of collector doping. The results demonstrate the impact of the valence band offset of **SiGe** heterojunctions on the **performance** of **PNP transistors**. 6 Refs.

30/3,AB/8 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02534752 Genuine Article#: LJ673 Number of References: 249
Title: STRAINED-LAYER HETEROSTRUCTURES, AND THEIR APPLICATIONS TO MODFETS, HBTS, AND LASERS (Abstract Available)
Author(s): MORKOC H; SVERDLOV B; GAO GB
Corporate Source: UNIV ILLINOIS,COORDINATED SCI LAB/URBANA//IL/61801
Journal: PROCEEDINGS OF THE IEEE, 1993, V81, N4 (APR), P493-556
ISSN: 0018-9219
Language: ENGLISH Document Type: REVIEW
Abstract: Recent developments in the art and technology of strained layer epitaxial systems are reviewed. This interest stems primarily from the additional degree of freedom that strained layers provide in the design of technologically important heterostructures and devices. This added degree of freedom has already led to device structures that can be tailored to a particular application with, in many cases, performances that are unparalleled and out of reach with lattice-matched systems alone. To date, modulation-doped field-effect transistors (MODFET's) fabricated with strained InGaAs channels on GaAs and InP substrates have shown superior performance over their counterparts with lattice-matched channels. MODFET's with unprecedented performance, e.g., a power gains of 7.3 dB at 140 GHz and a noise level of 1.4 dB in the 90-GHz range have been fabricated.

With the advent of **SiGe** alloys, the concept of strained layers was recently extended to include the elemental semiconductors as well. Heterojunctions formed in the **Si/SiGe** system have provided a laboratory in which to study quantum phenomena and explore heterojunction bipolar transistors (HBT's) and field-effect transistors (**FET's**). **SiGe** HBT's have already exhibited current gains in excess of 5000, current gain **cutoff frequencies** f(T) of about 75 GHz, and 24-ps switching times. Of particular significance are the recent reports of enhanced mobilities in strained **SiGe** and strained **Si** with applications to high-speed complementary **metal-oxide-semiconductor** (**CMOS**) circuits.

In the area of optoelectronics, quantum well lasers with compressively strained InGaAs active layers have led to considerable

reduction the threshold current density. Both compressive and tensile strains have been shown to lead to reduced threshold currents owing to favorable alterations in the valence-band structure. With coherently strained active layers based on GaAs, lasers with longevities superior to those with lattice-matched channels have been obtained. With strained channels the 0.98-mum wavelength radiation can be produced with important applications to Er-doped fiber amplifiers. Strained layer concepts have also been successfully used in yellow and green lasers made in InGaAlP and ZnCdSe/ZnSSe, respectively.

30/3,AB/9 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs

2311420 H.W. WILSON RECORD NUMBER: BAST01000301
High performance 0.1 mm gate-length **P-type SiGe** MODFET's and **MOS**-MODFET's
Lu, Wu; Kuliev, Almaz; Koester, Steven J
IEEE Transactions on Electron Devices v. 47 no8 (Aug. 2000) p. 1645-52
DOCUMENT TYPE: Feature Article ISSN: 0018-9383

ABSTRACT: The authors examined the characteristics of **p-type SiGe/Si** MODFETs and **MOS**-MODFETs with 0.1 mm gate length.
High-quality jet-vapor-deposited SiO2 was used as the gate dielectric for the **MOS**-MODFETs. The MODFET devices showed an intrinsic transconductance of 142 mS/mm, a unity current gain **cut-off frequency** of 45 **GHz**, and a maximum oscillation frequency of 81 GHz. The **MOS**-MODFETs showed a lower gate leakage current and a wider gate operating voltage swing in comparison to the MODFETs. Other characteristics of the devices are also described.

36/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015634694
WPI Acc No: 2003-696876/200366
XRAM Acc No: C03-191451
XRPX Acc No: N03-556564

Integrated circuit fabricated in semiconductor material of first conductivity type, and having **vertical** bipolar **transistor**(s) comprises layer of opposite conductivity type buried in semiconductor material of first conductivity type

Patent Assignee: SALLING C T (SALL-I); WU Z (WUZZ-I)
Inventor: SALLING C T; WU Z

Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030137029	A1	20030724	US 200251639	A	20020118	200366	B

Priority Applications (No Type Date): US 200251639 A 20020118
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030137029	A1		10	H01L-027/82	

Abstract (Basic): US 20030137029 A1
Abstract (Basic):

NOVELTY - An integrated circuit (300) fabricated in semiconductor material (301) of a first conductivity type, the circuit having at the surface a **vertical** bipolar **transistor**(s) comprises:

(i) a layer of the opposite conductivity type buried in the semiconductor material of the first conductivity type, as collector of the transistor having sharp junctions; and

(ii) a subsurface semiconductor band of the first conductivity type

DETAILED DESCRIPTION - An integrated circuit fabricated in semiconductor material of a first conductivity type, the circuit having at the surface a **vertical** bipolar **transistor**(s) surrounded at least in part by a dielectric isolation zone, comprises:

(a) a first surface region of opposite conductivity type, as an emitter(310, 311);

(b) a second surface region of the first conductivity type, as a base contact (312, 313);

(c) a well (371) of opposite conductivity type surrounding the first and second surface regions, extending from the surrounding deep into the semiconductor material of the first conductivity type;

(d) a layer of the opposite conductivity type buried in the semiconductor material of the first conductivity type, as collector of the transistor having sharp junctions;

(e) a subsurface semiconductor band of the first conductivity type between the layer and the surface and surrounded by the well, the band being the base of the transistor providing a width controlled, by the proximity of the buried layer (360) junction to the surface, and a resistivity higher than the remainder of the semiconductor material, thus enabling the **vertical** bipolar **transistor** to operate as a low breakdown voltage transistor for low electrostatic discharge (ESD) clamping voltage and high-beta.

The layer extends laterally to the wells, electrically isolating the base and emitter portions of the transistor from the remainder of the semiconductor material. It extends vertically from the surface regions, beginning at a level more shallow than the depth of the

dielectric isolation zone, and extending to a depth greater than the depth of the dielectric zone.

An INDEPENDENT CLAIM is also included for a method of fabricating, in a semiconductor region of a first conductivity type having two wells of the opposite conductivity type, a **vertical** bipolar **transistor**, comprising:

(1) depositing a photoresist layer (330), over the surface of the region and opening a window (330a) in the layer, exposing the surface area between the wells;

(2) implanting at low energy ions of the opposite conductivity type through the window, creating a shallow layer of the opposite conductivity under the surface; and

(3) implanting, at high energy and high dose (340), ions of the opposite conductivity type into the region of the first conductivity type through the window, creating a deep buried region having a net doping of the opposite conductivity type between, and connecting to the wells, as the collector of the transistor, and further creating a near-surface region of the first conductivity type, having a doping concentration lower than that of the remainder of the region, being the base of the transistor.

USE - Used as integrated circuit, e.g. **metal-oxide-semiconductor** integrated circuits, useful in electronic systems.

ADVANTAGE - The method is coherent and of low-cost, enhancing ESD insensitivity without the need for additional, real-estate consuming protection devices. It is simple, yet flexible enough for different semiconductor product families and a wide spectrum of design and process variations. The device structure provides for excellent electrical **performance**, mechanical stability and **high** reliability. No investment in new manufacturing machines is needed. The substrate resistance is increased as a welcome side effect of the fabrication of the collector by ion implantation. The collector has a low breakdown voltage, and thus low ESD clamping voltage. A **silicon** area-saving **vertical transistor**, is created, without an additional photomask step.

DESCRIPTION OF DRAWING(S) - The figure is a schematic cross section of a **vertical** bipolar **transistor** with buried collector.

Integrated circuit (300)
Semiconductor material (301)
Inner pair (302)
Emitter (310, 311)
Base contact (312, 313)
Photoresist layer (330)
Window (330a)
High energy and high dose (340)
Buried layer (360)
Outer pair (370)
Wells (371)
pp; 10 DwgNo 3/3

37/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7176081 INSPEC Abstract Number: B2002-03-2560J-016
Title: **High performance** 0.25 mu m **SiGe** and **SiGe**:C HBTs using non selective epitaxy
Author(s): Baudry, H.; Martinet, B.; Fellous, C.; Kermarrec, O.; Campidelli, Y.; Laurens, M.; Marty, M.; Mourier, J.; Troillard, G.; Monroy, A.; Dutartre, D.; Bensahel, D.; Vincent, G.; Chantre, A.
Author Affiliation: Centre Commun. de Microelectronique de Crolles, ST Microelectron., Crolles, France
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting (Cat. No.01CH37212) p.52-5
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 199 pp.
ISBN: 0 7803 7019 8 Material Identity Number: XX-2001-02296
U.S. Copyright Clearance Center Code: 0-7803-7019-8/01/$10.00
Conference Title: Proceedings of the 2001 BIPOLAR/BiCMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron. Devices Society; IEEE Solid-State Circuits Society; IEEE Twin Cities Sect
Conference Date: 30 Sept.-2 Oct. 2001 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: A robust 0.25 mu m double-poly **SiGe** HBT structure using non selective epitaxy has been developed. The device features 70/90 GHz f/sub T//f/sub max/ with pure **SiGe** base in 0.25 mu m **BiCMOS** technology. Performances up to 120/100 GHz f/sub T//f/sub max/ are demonstrated for **SiGe**:C base transistors.
Subfile: B

37/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7081261 INSPEC Abstract Number: B2001-12-2560R-048
Title: **Ge**-redistributed poly-**Si/SiGe** stack gate (GRPSG) for **high-performance** CMOSFETs
Author(s): Rhee, H.S.; Bae, G.J.; Choe, T.H.; Kim, S.S.; Song, S.; Lee, N.I.; Fujihara, K.; Kang, H.K.; Moon, J.T.
Author Affiliation: Semicond. R&D Div., Samsung Electron. Co. Ltd., Yongin, South Korea
Conference Title: 2001 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.01 CH37184) p.61-2
Publisher: Japan Society Appl. Phys, Tokyo, Japan
Publication Date: 2001 Country of Publication: Japan xv+150 pp.
ISBN: 4 89114 012 7 Material Identity Number: XX-2001-01380
Conference Title: 2001 Symposium on VLSI Technology. Digest of Technical Papers
Conference Date: 12-14 June 2001 Conference Location: Kyoto, Japan
Language: English
Abstract: A **Ge**-redistributed poly-**Si/SiGe** stack gate (GRPSG) has been proposed to improve the current performance of **PMOS** without the degradation of **NMOS** for sub-0.1 mu m CMOSFETs with ultrathin gate oxide. **Ge** diffusion into the poly-**Si** layer was promoted more by ion implantation of **N-type** dopants such as P and As rather than **P-type** dopants. **NMOS** and **PMOS**

had different **Ge** concentrations at the interface between gate electrode and gate oxide by an additional anneal to redistribute the **Ge** profile. The current performance of **NMOS** with GRPSG with low **Ge** content (<5%) was not degraded, while that of **PMOS** with GRPSG with high **Ge** content (>20%) was improved due to suppression of the poly-depletion effect and boron penetration. In addition, the gate reoxidation was modified to reduce G/sub m/ degradation by reduced gate bird's beak. **High-performance** 70 nm-CMOSFETs were successfully fabricated using the simple GRPSG process.

Subfile: B

37/3,AB/3 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

6562453 INSPEC Abstract Number: B2000-05-2570D-017

Title: **High-performance** deep submicron **CMOS** technologies with polycrystalline-**SiGe** gates

Author(s): Ponomarev, Y.V.; Stolk, P.A.; Salm, C.; Schmitz, J.; Woerlee, P.H.

Author Affiliation: Philips Res. Laboratory, Eindhoven, Netherlands

Journal: IEEE Transactions on Electron Devices vol.47, no.4 p. 848-55

Publisher: IEEE,

Publication Date: April 2000 Country of Publication: USA

CODEN: IETDAI ISSN: 0018-9383

SICI: 0018-9383(200004)47:4L.848:HPDS;1-8

Material Identity Number: I037-2000-004

U.S. Copyright Clearance Center Code: 0018-9383/2000/$10.00

Language: English

Abstract: The use of polycrystalline **SiGe** as the gate material for deep submicron **CMOS** has been investigated. A complete compatibility to standard **CMOS** processing is demonstrated when polycrystalline **Si** is substituted with **SiGe** (for **Ge** fractions below 0.5) to form the gate electrode of the transistors. Performance improvements are achieved for **PMOS** transistors by careful optimization of both transistor channel profile and **p-type** gate workfunction, the latter by changing **Ge** mole fraction in the gate. For the 0.18 mu m **CMOS** generation we record up to 20% increase in the current drive, a 10% increase in the channel transconductance and subthreshold swing improvement from 82 mV/dec to 75 mV/dec resulting in excellent "on"/"off" currents ratio. At the same time, **NMOS** transistor performance is not affected by gate material substitution.

Subfile: B

37/3,AB/4 (Item 4 from file: 2)

DIALOG(R)File 2:INSPEC

5802340 INSPEC Abstract Number: B9802-2570D-053

Title: Gate-workfunction engineering using poly-(**Si**,**Ge**) for **high-performance** 0.18 mu m **CMOS** technology

Author(s): Ponomarev, Y.V.; Salm, C.; Schmitz, J.; Woerlee, P.H.; Stolk, P.A.; Gravesteijn, D.J.

Author Affiliation: MESA Res. Inst., Twente University, Enschede, Netherlands

Conference Title: International Electron Devices Meeting 1997. IEDM

Technical Digest (Cat. No.97CH36103) p.829-32
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 944 pp.
ISBN: 0 7803 4100 7 Material Identity Number: XX97-03283
U.S. Copyright Clearance Center Code: 0 7803 4100 7/97/$10.00
Conference Title: International Electron Devices Meeting. IEDM Technical Digest
Conference Sponsor: Electron Devices Society IEEE
Conference Date: 7-10 Dec. 1997 Conference Location: Washington, DC, USA
Language: English
Abstract: We show that poly-**SiGe** can be readily integrated as a gate material into an existing **CMOS** technology to achieve significant increase in the transistor performance. In order to preserve the standard salicidation scheme, a buffer poly-**Si** layer is introduced in the gate stack. **PMOST** channel profiles are optimized to account for the change of the gate workfunction. **High-performance CMOS** 0.18 mu m devices are manufactured using p- and **n-type** poly-**Si**/**Si**/sub 0.8/**Ge**/sub 0.2/ gates.
Subfile: B

37/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

5285698 INSPEC Abstract Number: B9607-2560R-070
Title: Super self-aligned ultrashallow junction formation using selective **Si**/sub 1-x/**Ge**/sub x/ CVD in deep-submicron **MOSFETs** fabrication
Author(s): Goto, K.; Murota, J.; Honma, F.; Matsuura, T.; Sawada, Y.
Author Affiliation: Laboratory for Electron. Intelligent Syst., Tohoku University,
Sendai, Japan
Conference Title: Proceedings of the Fifth International Symposium on Ultra Large Scale Integration Science and Technology. ULSI Science and Technology / 1995 p.512-18
Editor(s): Middlesworth, E.M.; Massoud, H.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1995 Country of Publication: USA ix+533 pp.
Material Identity Number: XX95-02965
Conference Title: Proceedings of Fifth International Symposium. ULSI Science and Technology
Conference Sponsor: Electrochem. Soc
Conference Date: 23-26 May 1995 Conference Location: Reno, NV, USA
Language: English
Abstract: In order to prevent the short channel effects of deep submicron **MOSFETs**., a novel super self-aligned ultrashallow junction formation was proposed. Using an ultraclean LPCVD system and an optimized sequence, selective deposition of B-doped **Si**/sub 1-x/**Ge**/sub x/ on **n**-**type** **Si** and a **high performance** ultrashallow p/sup +/n junction have been realized. **pMOSFETs** were fabricated using this selective B-doped **Si**/sub 0.5/**Ge** /sub 0.5/ for self-aligned ultrashallow source/drain regions, and they showed a much smaller threshold voltage shift compared with the same size B/sup +/-implanted **MOSFETs**.
Subfile: B

37/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

4827040 INSPEC Abstract Number: B9501-0510D-017
Title: UHVCVD growth of **Si/SiGe** heterostructures and their applications
Author(s): Meyerson, B.S.; Ismail, K.E.; Harame, D.L.; LeGoues, F.K.; Stork, J.M.C.
Author Affiliation: Res. Div., IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: Semiconductor Science and Technology vol.9, no.11S p. 2005-10
Publication Date: Nov. 1994 Country of Publication: UK
CODEN: SSTEET ISSN: 0268-1242
U.S. Copyright Clearance Center Code: 0268-1242/94/112005+06$19.50
Conference Title: Eighth International Winterschool on New Developments in Solid State Physics
Conference Date: 14-18 Feb. 1994 Conference Location: Mauterndorf, Austria
Language: English
Abstract: The era of integrated circuits based on **SiGe** heterojunction bipolar transistors arrived with the announcement of a 12-bit digital to analogue converter (DAC) fabricated using an analogue optimization of IBM's **SiGe** HBT technology. Medium-scale integration was employed, the circuit consisting of approximately 3000 transistors and 2000 passive elements (resistor and capacitors). Operable at 1 GHz, this converter consumes approximately 0.75 W, thus yielding power-delay performance a decade superior to prior devices. It is significant that this DAC was fabricated employing the same technology and toolset as found on a standard **silicon**-based **CMOS** product line. In addition to the **CMOS** toolset, only one unique tool is required to support this technology, a commercial (Leybold-AG) ultrahigh vacuum chemical vapour deposition system for **SiGe** deposition. It is of interest to note, however, that the processing of these integrated circuits was no different from that employed in fabricating **high-performance SiGe high** electron mobility transistors (HEMTs), as well as the first **N-type SiGe**-based resonant tunnelling devices (RTDs), all functional at room temperature. This enables one to combine a wafer-scale manufacturable **SiGe**-based heterojunction technology with devices that utilize quantum phenomena, made accessible by the use of band offsets and strain-induced band splitting in the **Si/SiGe** materials system. This new ability to incorporate leading edge developments in **SiGe** device physics into a standard technology line opens up a host of new areas for exploration.
Subfile: B

37/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

04111470 INSPEC Abstract Number: B9204-2570K-010
Title: A CRYO-**BiCMOS** technology with **Si/SiGe** heterojunction bipolar transistors
Author(s): Imai, K.; Yamazaki, T.; Tashiro, T.; Tatsumi, T.; Niino, T.; Aizaki, N.; Nakamae, M.
Author Affiliation: NEC Corp., Kanagawa, Japan
Conference Title: Proceedings of the 1990 Bipolar Circuits and Technology

Meeting (Cat. No.90CH2890-2) p.90-3
Editor(s): Jopke, J.
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA 262 pp.
Conference Sponsor: IEEE
Conference Date: 17-18 Sept. 1990 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: A **high-performance** liquid-nitrogen temperature **BiCMOS** (CRYO-**BiCMOS**) technology with **Si/SiGe** heterojunction bipolar transistors (HBTs) is presented. The newly developed HBT, ..., which has an n/sup +/-polysilicon/**n-type Si** epitaxial layer emitter structure on a **p-type SiGe** base layer, shows a high current gain of 50 at liquid nitrogen temperature. Under the conditions of 3.3 V and 83 K, the driving capability of CRYO-**BiCMOS** gates is two times larger than that of the CRYO-**CMOS** gate. At 3.3 V and a load capacitance of 1 pF, the gate delay of CRYO-**BiCMOS** gate with pull-up HBT is 480 ps. The CRYO-**BiCMOS** with **Si/SiGe** HBTs presented is very promising for the future progress of **BiCMOS** LSIs.
Subfile: B

37/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

01741465 INSPEC Abstract Number: A81086663, B81040421
Title: Amorphous **SiGe**:H for **high performance** solar cells
Author(s): Nakamura, G.; Sato, K.; Yukimoto, Y.; Shirahata, K.; Murahashi, T.; Fujiwara, K.
Author Affiliation: LSI Res. & Dev. Laboratory, Mitsubishi Electric Corp., Mizuhara, Itami, Japan
Journal: Japanese Journal of Applied Physics vol.20, suppl.20-1 p. 291-6
Publication Date: 1981 Country of Publication: Japan
CODEN: JJAPA5 ISSN: 0021-4922
Conference Title: Twelfth Conference on Solid State Devices
Conference Date: 26-27 Aug. 1980 Conference Location: Tokyo, Japan
Language: English
Abstract: A preliminary study has been carried out on electrical and optical properties of films deposited by a glow discharge plasma reaction. As the **germanium** content in the film increases, the optical absorption coefficient increases and the optical gap energy E/sub g/opt. decreases. The growth rate of a-**SiGe**:H films increases with the **germanium** content and reaches a value for pure a-**Ge**:H films about 3 times larger than that of a pure a-**Si**:H film. Film properties were examined by dark- and photoconductivity, **MOSFET** transistor characteristics, and photoluminescence. Photoconductivity and carrier mobilities decrease drastically when the mole ratio GeH/sub 4//(GeH/sub 4/+SiH/sub 4/) exceeds 25%. Solar cells of various structures using a-**SiGe**:H and a-**Si**:H films were fabricated and their photovoltaic properties compared with that of a simple p-i-**n type** a-**Si**:H solar cell. Tandem structures with a-**Si**:H p-i-n and a-**SiGe**:H p-i-n cells show a broadened spectral response in the long wavelength region and an open circuit voltage of 1.13 V, about twice that of a single cell.
Subfile: A B

37/3,AB/9 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05590274 Genuine Article#: WJ494 Number of References: 25
Title: Suppression of the floating-body effect in SOI **MOSFET**'s by the bandgap engineering method using a Si1-xGex source structure (ABSTRACT AVAILABLE)
Author(s): Yoshimi M (REPRINT) ; Terauchi M; Nishiyama A; Arisumi O; Murakoshi AR; Matsuzawa K; Shigyo N; Takeno S; Tomita M; Suzuki K; Ushiku Y; Tango H
Corporate Source: TOSHIBA CO LTD,ULSI, RES LABS, R&D CTR/KAWASAKI/KANAGAWA 210/JAPAN/ (REPRINT); TOSHIBA CO LTD,MICROELECT ENGN LAB/KAWASAKI/KANAGAWA 210/JAPAN/; TOSHIBA CO LTD,ENVIRONM ENGN LAB, R&D CTR/KAWASAKI/KANAGAWA 210/JAPAN/
Journal: IEEE TRANSACTIONS ON ELECTRON DEVICES, 1997, V44, N3 (MAR), P 423-430
ISSN: 0018-9383 Publication date: 19970300
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: ARTICLE
Abstract: The bandgap engineering method using a **SiGe** source structure is presented as a means to suppress the floating-body effect in SOI **MOSFET**'s. Experiments using **Ge** implantation are carried out to form a narrow-bandgapped **SiGe** layer in the source region. It has been confirmed that **Ge**-implanted SIMOX exhibited a 0.1 eV bandgap narrowing with a relatively low **Ge**-dosage of 10(16) cm(-2). The fabricated **N-type** SOI-**MOSFET**'s exhibited suppressed parasitic bipolar effects, such as improvement of the drain breakdown voltage or latch voltage, and suppression of abnormal subthreshold slope. Advantages over other conventional methods are also discussed, indicating that the bandgap engineering provides a practical method to suppress the floating-body effect.

37/3,AB/10 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

02284536 Genuine Article#: KQ003 Number of References: 8
Title: FABRICATION OF A SI1-XGEX CHANNEL **METAL-OXIDE-SEMICONDUCTOR** FIELD-EFFECT TRANSISTOR (**MOSFET**) CONTAINING HIGH **GE** FRACTION LAYER BY LOW-PRESSURE CHEMICAL VAPOR-DEPOSITION (Abstract Available)
Author(s): GOTO K; MUROTA J; MAEDA T; SCHUTZ R; AIZAWA K; KIRCHER R; YOKOO K; ONO S
Corporate Source: TOHOKU UNIV,ELECT COMMUN RES INST,MICROELECTR LAB,2-1-1 KATAHIRA,AOBA KU/SENDAI/MIYAGI 980/JAPAN/
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS & SHORT NOTES, 1993, V32, N1B (JAN), P438-441
ISSN: 0021-4922
Language: ENGLISH Document Type: ARTICLE
Abstract: A method for growing the high-quality strained epitaxial heterostructure of **Si**/Si1-xGex/**Si** by low-pressure chemical vapor deposition (CVD) and the fabrication of Si1-xGex-channel **metal-oxide-semiconductor** field-effect transistors (**MOSFET**'s) with a high **Ge** fraction layer have been investigated. It is found that lowering of the deposition temperature of the Si1-xGex and **Si** capping layers is necessary with increasing **Ge** fraction in order to prevent island growth of the

layers. With the use of the optimized fabrication process, **Si** /Si1-xGex/**Si** heterostructures with flat surfaces and interfaces were realized, and a **high-performance** Si0.5Ge0.5-channel **MOSFET** has been achieved with a large mobility enhancement of about 70% at 300 K and over 150% at 77 K compared with that of a **MOSFET** without a Si1-xGex channel.

37/3,AB/11 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01737301 AADAAI0801272
Technology for **SiGe** heterostructure-based **CMOS** devices
Author: Armstrong, Mark Albert
Degree: Ph.D.
Year: 1999
Corporate Source/Institution: Massachusetts Institute of Technology (0753)
Source: VOLUME 61/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 1542.

Bulk silicon is currently the substrate material of choice for the manufacture of **high-performance** digital circuits due to its highly-developed processing technology and the relatively low cost for high-quality substrates. Silicon-based **MOSFETs** have reached remarkable levels of performance through device scaling. However, with each technology generation, it is becoming harder and harder to improve device performance at the same pace through traditional scaling methods alone. Short-channel effects such as velocity saturation and drain-induced barrier lowering have placed an fundamental limit on the ultimate performance of bulk Si **MOSFETS**.

One way to raise this limit is to increase the carrier mobilities in the channel. This can be done using high-mobility Si and **SiGe** strained-layers. Unlike III-V-based high-mobility materials, Si/**SiGe** strained-layers have the advantage of being largely compatible with mainstream Si processing, which is important from a financial feasibility standpoint. This thesis examines several issues related to Si/**SiGe** strained-layer devices and their integration into mainstream **CMOS**.

The first part of this work strives to predict the **performance** leverage of **high**-mobility Si/**SiGe** over bulk Si devices and circuits in a realistic manner. Two-dimensional hydrodynamic simulations are used to predict static device characteristics including effects of series resistance, velocity saturation and velocity overshoot. The simulations show enhanced current drive over bulk Si devices at 0.2 μm effective channel length and high-light the importance of velocity overshoot in high-mobility submicron devices. The circuit performance of Si/**SiGe** devices is determined from transient simulations of **CMOS** ring oscillators including the effects of parasitic capacitance and drain-to-source voltage at the onset of saturation V_{DS,sat}. The simulations show a 4 to 6-fold reduction in power-delay product as compared to bulk **CMOS** oscillators operated at 2.5 V with the same design rules.

The remainder of the thesis focuses on the fabrication and characterization of strained-Si **NMOS** devices. The vehicle for this work is a novel short-flow, single-mask **MOSFET** which can be fabbed in as little as a week. This device is superior to simple Hall mobility structures which suffer from leakage through the substrate, an inability to control the carrier concentration and the uncertainty associated with the Hall scattering factor.

I investigate a novel buried-channel strained-Si **NMOS** structure incorporating an **n-type** donor layer beneath the strained-Si channel to encourage occupation of the buried channel and increase the overall mobility. Peak mobility in a structure without a donor layer reproduces the best results in the literature for buried-channel strained-Si **NMOS** devices. For structures with donor layers, Coulomb scattering from charges in the donor layer eradicates any benefit from increased buried-channel occupation.

I also investigate the effect of well implants on the mobility of surface-channel strained-Si **NMOS** devices. Similar to the universal mobility curve in bulk Si, mobility at low perpendicular electric field degrades with increasing implant dose while high field mobility is unaffected. The mobility is largely unaffected by a neutral implant species at the same dose. This leads to the conclusion that the material quality of the strained-layer is not affected by the implant, and that the mobility degradation is due solely to increased ionized impurity scattering. (Copies available exclusively from MIT Libraries, Rm. 14-0551, Cambridge, MA 02139-4307. Ph. 617-253-5668; Fax 617-253-1690.)

37/3,AB/12 (Item 2 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01367234 AAD9422097
APPLICATIONS OF POLYCRYSTALLINE **SILICON-GERMANIUM** THIN FILMS IN **METAL-OXIDE-SEMICONDUCTOR** TECHNOLOGIES

Author: KING, TSU-JAE
Degree: PH.D.
Year: 1994
Corporate Source/Institution: STANFORD UNIVERSITY (0212)
Source: VOLUME 55/03-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 1088. 151 PAGES

Polycrystalline **silicon** (poly-**Si**) is an important component of **silicon** integrated-circuit (IC) technology and is currently used in a wide range of device applications. The fundamental properties of **silicon-germanium** (**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$) indicate that poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ can be a favorable alternative to poly-**Si** in many of these applications. Since the melting point of **Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ is lower than that of **Si**, physical phenomena controlling fabrication processes such as deposition, crystallization, and dopant activation occur at lower temperatures for **Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ than for **Si**. Thus, lower process temperatures can be used for poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x},$ so that it is preferable to poly-**Si** for various applications in technologies which have limited thermal-budget allowances. In this work, a deposition technology for poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ films has been developed, and the physical and electrical properties of these films have been characterized. Two important potential applications of poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ films in **metal-oxide-semiconductor** (**MOS**) technologies have been investigated: first, the application as a gate-electrode material; second, the application as a thin-film transistor (TFT) channel material. The resistivity of heavily doped **p-type** (p$\sp+$) poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ is lower than that of comparably doped poly-**Si**, and its work function can be easily modified by adjusting its **germanium** content. These properties make p$\sp+$ poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ a very attractive candidate for

the gate-electrode material in submicrometer complementary **MOS** (**CMOS**) technologies. p-channel TFTs fabricated in poly-**Si** $\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ exhibit well-behaved device characteristics and may be suitable for high-density static memory (SRAM) and three-dimensionally integrated circuit applications. n- and p-channel poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ TFTs have been successfully fabricated using conventional microelectronic fabrication techniques without exceeding 550$\sp\circ$C. This demonstrated low-temperature-processing capability permits the fabrication of **high -performance CMOS** circuits on glass substrates using a process no more complex than that for fabricating **silicon** TFTs. Therefore, a poly-**Si**$\sb{\rm 1-x}$**Ge**$\sb{\rm x}$ TFT technology is particularly attractive for large-area electronics applications.

37/3,AB/13 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

03795324 INSIDE CONFERENCE ITEM ID: CN039883510
Electrical stress characteristics in **MOS** capacitors with **p-type** poly-**SiGe** and poly-Si gates in the direct tunneling regime" Physical Electronics and photonics, Microtechnology Centre at Chalmers (MC2), Physics Dept, Chalmers University of Technology and Goteborg University, S-412 96 Goteborg, Sweden
Yousif, M. Y. A.; Willander, M.; Lundgren, P.; Caymax, M.
CONFERENCE: High performance electron devices for microwave and optoelectronic applications-International symposium; 8th
EDMO -CONFERENCE-, 2000; 8TH P: 271-275
IEEE, 2000
ISBN: 078036550X
LANGUAGE: English DOCUMENT TYPE: Conference Preprinted papers
CONFERENCE SPONSOR: IEEE
IEE
University of Glasgow
CONFERENCE LOCATION: Glasgow 2000; Nov (200011) (200011)
NOTE:
Also known as EDMO 2000. IEEE cat no 00TH8534

37/3,AB/14 (Item 2 from file: 65)
DIALOG(R)File 65:Inside Conferences

03795275 INSIDE CONFERENCE ITEM ID: CN039883028
n-and **p-type** Si/**SiGe** Hetero **FETs**" Daimler Chrysler Research Labs, Ulm, Germany
Koenig, U.
CONFERENCE: High performance electron devices for microwave and optoelectronic applications-International symposium; 8th
EDMO -CONFERENCE-, 2000; 8TH P: 1-7
IEEE, 2000
ISBN: 078036550X
LANGUAGE: English DOCUMENT TYPE: Conference Preprinted papers
CONFERENCE SPONSOR: IEEE
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University of Glasgow
CONFERENCE LOCATION: Glasgow 2000; Nov (200011) (200011)
NOTE:
Also known as EDMO 2000. IEEE cat no 00TH8534

37/3,AB/15 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus
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02567702 JICST ACCESSION NUMBER: 95A0814987 FILE SEGMENT: JICST-E
Self-Aligned Ultrashallow Junction Formation Using Selective Si1-xGexCVD for Ultra-Small **MOSFET**.
GOTO KIN'YA (1); MUROTA JUN'ICHI (1); HONMA FUMITAKA (1); MATSUURA TAKASHI (1); SAWADA KOJI (1)
(1) Res. Inst. of Electr. Commun., Tohoku University
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1995, VOL.95,NO.205(SDM95 93-101), PAGE.9-14, FIG.8, REF.6
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In order to prevent the short channel effects of deep submicron **MOSFET**'s, novel super self-aligned ultrashallow junction formation was proposed. Using an ultraclean LPCVD system and an optimized sequence, selective deposition of B-doped Si1-xGex on **n -type Si** and a **high performance** ultrashallow p+n junction have been realized. **pMOSFET**'s were fabricated using this selective B-doped Si0.5Ge0.5 for self-aligned ultrashallow source/drain regions, and they showed a much smaller threshold voltage shift compared with the same size B+-implanted **MOSFET**'s. (author abst.)

37/3,AB/16 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
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2531024 H.W. WILSON RECORD NUMBER: BAST02145735
Series resistance and mobility degradation factor in C-incorporated **SiGe** heterostructure **p-type metal-oxide semiconductor** field-effect transistors
Kar, G. S; Maikap, S; Banerjee, S. K
Semiconductor Science & Technology v. 17 no9 (Sept. 2002) p. 938-41
DOCUMENT TYPE: Feature Article ISSN: 0268-1242

ABSTRACT: The authors developed **p-type MOSFET** devices with channel lengths from 0.8-10 mm. The devices were fabricated on strained **Si**/Si0.8Ge0.2/**Si** and partially strain-compensated **Si**/Si0.793Ge0.2C0.007/**Si** heterolayers. Below 160 K, the resulting ternary devices exhibited a sharp rise in source-drain resistance and in their mobility degradation factor. Results indicated that a **higher performance** level for ternary devices could be achieved, compared to **Si** and **SiGe** binary devices, by optimizing the source/drain contact metallization. However, performance enhancement at low temperatures was limited by alloy scattering and surface roughness in the ternary layer.

37/3,AB/17 (Item 1 from file: 350)

DIALOG(R)File 350:Derwent WPIX

015378631
WPI Acc No: 2003-439569/200341
Related WPI Acc No: 2002-656479; 2003-439715
XRAM Acc No: C03-116411
XRPX Acc No: N03-350761
Thin film transistor for image display device, includes insulator substrate, poly-crystalline thin film, and transistor, where poly-crystalline film in channel part is composed of **silicon-germanium** poly-crystalline
Patent Assignee: HATANO M (HATA-I); PARK S (PARK-I); SHIBA T (SHIB-I); YAMAGUCHI S (YAMA-I)
Inventor: HATANO M; PARK S; SHIBA T; YAMAGUCHI S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030049892	A1	20030313	US 2001790545	A	20010223	200341 B
			US 2002277140	A	20021022	

Priority Applications (No Type Date): JP 200125531 A 20010201
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030049892	A1		20	H01L-021/00	Div ex application US 2001790545

Abstract (Basic): US 20030049892 A1
Abstract (Basic):

NOVELTY - A thin film transistor comprises an insulator substrate; a poly-crystalline thin film formed on the insulator substrate; and a transistor composed of a source, a drain, a channel, and a gate (6) formed on the poly-crystalline thin film. The poly-crystalline film in the channel part is composed of a **silicon-germanium** poly-crystalline.

DETAILED DESCRIPTION - A thin film transistor comprises an insulator substrate; a poly-crystalline thin film formed on the insulator substrate; and a transistor composed of a source, a drain, a channel, and a gate formed on the poly-crystalline thin film. The poly-crystalline film in a channel part of the transistor is composed of a **silicon (Si)-germanium (Ge)** poly-crystalline (Si1-xGex), a ratio ox of a **germanium** composition relative to **silicon** is x lesser than 1 but greater than 0, and a ratio x of a **Ge** composition in the poly-crystalline thin film is larger in a grain boundary than a portion where a **Ge** eomposition in an interior grain of crystal becomes the minimum.

INDEPENDENT CLAIMS are also included for:

(a) a method for producing a thin film transistor device; and

(b) an image display device comprising an image display part, an image display circuit controlling a display of the image display part and including a data driver, a gate driver, and a buffer amplifier, and a peripheral circuit part in the neighborhood of the image display circuit and controlling the image display circuit, the circuit part including a complementary **metal oxide semiconductor** type transistor making present as a mixture of **p-type** and/or **n-type** transistor.

USE - The invention is used for an image display device (claimed).

ADVANTAGE - The invention provides an image display device having **high performance**, and a large area with low cost.

DESCRIPTION OF DRAWING(S) - The figure shows the thin film transistor.

Gate (6)
pp; 20 DwgNo 4/12

37/3,AB/18 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010357578
WPI Acc No: 1995-258892/199534
XRAM Acc No: C95-117925
XRPX Acc No: N95-199471
Semiconductor element e.g. **FET** - has mixed crystal layer of 10 microns width arranged parallel to surface bearing of substrate
Patent Assignee: HITACHI LTD (HITA)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7162015	A	19950623	JP 93310548	A	19931210	199534	B

Priority Applications (No Type Date): JP 93310548 A 19931210
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7162015	A		6	H01L-029/80	

Abstract (Basic): JP 7162015 A

The semiconductor element comprises a **p type Si** substrate with a surface bearing of (100). Over the substrate, a **Si**(1-X) GeX mixed crystal layer is formed parallel to the surface bearing of the substrate. The layer width of the mixed crystal layer is lesser than or equal to 10 micrometers.

ADVANTAGE - Facilitates increase in **germanium** density without producing any transposition. Enlarges band discontinuity between substrate and mixed crystal layer to twice original value. Lowers average effective mass of electrons. Raises **high** speed **performance** to thrice original value. Lowers defect generation rate without lowering mixed crystal ratio.

Dwg.1/6

37/3,AB/19 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

07029640
SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

PUB. NO.: 2001-257274 [JP 2001257274 A]
PUBLISHED: September 21, 2001 (20010921)
INVENTOR(s): HISAMOTO MASARU
KACHI TAKESHI
APPLICANT(s): HITACHI LTD
APPL. NO.: 2000-069778 [JP 200069778]
FILED: March 14, 2000 (20000314)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance CMOS** with a little parasitic resistance.

SOLUTION: The **CMOS** is constituted such that **p-type**

impurity diffused electrodes 310 constituting source and drain regions of **pMOSs** are electrically connected to a metal wiring layer 600 through a **p-type** polycrystalline **silicon-** made leading layer 300, and **n-type** impurity diffused electrodes 410 constituting source and drain regions of **nMOSs** are electrically connected to the metal wiring layer 600 through an **n-type silicon-germanium** mixed crystal-made leading layer 400. The p- and **n-type** leading layers 300, 400 are formed by selectively etching off only either the polycrystalline **silicon** or **silicon-germanium** mixed crystal, utilizing a high etching selective ratio of both.

37/3,AB/20 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

05906515
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 10-189615 [JP 10189615 A]
PUBLISHED: July 21, 1998 (19980721)
INVENTOR(s): EJIRI YOICHI
APPLICANT(s): SONY CORP [000218] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-342925 [JP 96342925]
FILED: December 24, 1996 (19961224)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **high-performance, high-density, high** -integration and high-reliability LSI device by a method wherein the performances of many semiconductor devices including a bipolar transistor, which has a low base resistance are enhanced without reducing its reliability and yield.

SOLUTION: A bipolar transistor 1 is provided with a base lead-out electrode 31, which is connected with a **silicon** layer 13 and made of an alloy **silicon** and a high-melting point metal, such as a tungsten silicide layer. In this case, **germanium**-containing semiconductor layers 17 are respectively provided in the interfaces between graft base layers 34, which are **P-type** semiconductor layers formed in parts of the layer 13, and the electrode 31, whereby the tungsten silicide layer does not absorb boron.

37/3,AB/21 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO

05809925
SEMICONDUCTOR DEVICE

PUB. NO.: 10-093025 [JP 10093025 A]
PUBLISHED: April 10, 1998 (19980410)
INVENTOR(s): HIRAOKA YOSHIKO
KUROBE ATSUSHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 08-245317 [JP 96245317]
FILED: September 17, 1996 (19960917)

ABSTRACT

PROBLEM TO BE SOLVED: To realize **high** speed and **high performance** by well consistently forming **high-performance** Si **type** n- and p-channel hetero-junction **FETs** on a substrate.

SOLUTION: A complementary inverter has n- and p-channel hetero-junction **FETs** on a substrate. On the Si substrate 30 are laminated a first semiconductor layer 31 made of a lattice-relaxed **SiGe** to form an electron feed layer, second semiconductor layer 32 made of a tensile-strained Si to form an electron-channel layer and hole feed layer and third semiconductor layer 33, made of a lattice- relaxed **SiGe** to form a hole channel 1. On a part of the third layer 33 gate electrodes 36 and source-drain electrodes 37 are formed to construct the p- channel heterojuction **FETs**. The third layer 33 is removed, gate electrodes 34 and source-drain electrodes 35 are formed on the exposed second layer 32 to form the n-channel heterojuction **FETs**.

37/3,AB/22 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO

04299602
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 05-291302 [JP 5291302 A]
PUBLISHED: November 05, 1993 (19931105)
INVENTOR(s): OKAMOTO AKIHIKO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 04-084285 [JP 9284285]
FILED: April 07, 1992 (19920407)
JOURNAL: Section: E, Section Number 1505, Volume 18, Number 80, Pg. 3, February 09, 1994 (19940209)

ABSTRACT

PURPOSE: To prevent an electric field from concentrating on the end of a gate and then to obtain a **high-performance FET** of the reduced source resistance by changing only a non-doped region between a source electrode and a gate electrode into an **n-type** semiconductor by ion implantation.

CONSTITUTION: A high-purity GaAs layers 1-3 are caused to grow on a semi-insulating GaAs substrate 6 by the molecular beam epitaxial method. Then, an **n-type** GaAs layer 4 is caused to grow. Nextly, a part of the epitaxial layers is removed by etching and the non-doped layer is etched to make it a recess- having structure and then a gate electrode 8 is formed with heat resistant metal. After that, the whole surface is coated with resist 10. After selectively removing the resist only at the source side, **silicon**, an **n-type** impurity, is doped by ion implantation. Nextly, a part of the resist is opened for a source and a drain and then the source and the drain electrode are formed with gold-**germanium** - nickel allay by evaporation. By this method, a source resistance of **FET** can be reduced and a high drain withstand voltage can be maintained and eventually characteristics of the high output **FET**, etc., can be enhanced.

37/3,AB/23 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO

03617537
SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

PUB. NO.: 03-280437 [JP 3280437 A]
PUBLISHED: December 11, 1991 (19911211)
INVENTOR(s): NAKAGAWA AKIO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-078905 [JP 9078905]
FILED: March 29, 1990 (19900329)
JOURNAL: Section: E, Section Number 1177, Volume 16, Number 101, Pg. 165, March 12, 1992 (19920312)

ABSTRACT

PURPOSE: To contrive an increase in the performance of a semiconductor device utilizing a heterojunction structure by a method wherein a channel region under a gate insulating film is constituted of an **SiGe** layer.

CONSTITUTION: The p(sup +) source and drain diffused layers 6 and 7, which are isolated from each other, are formed in an **n-type Si** substrate 1 and a gate electrode 5 is formed on the substrate surface between the layers 6 and 7 via a gate insulating film 4. The film 4 is a thermal oxide film and the electrode 5 is a polycrystalline **silicon** film. An **SiGe** layer 2 is formed at a part, which is used as a channel region, under the film 4 by an ion implantation of **Ge**. A thin **Si** layer 3 is left on the layer 2. The layer 2 if formed in such a way that both ends intrude into the layers 6 and 7. As the layer 2 which is formed as the channel region if formed in the interior, which is positioned more inside than the interface between the film 4 and the substrate, of the substrate, a carrier mobility in the channel region is increased by a principle identical with that of an HEMT and **high-performance** field-effect element characteristics are obtained. As the **Si** substrate is used, a thin gate insulating film consisting of an oxide film of good quality can be formed by a thermal oxidation and an element having a high gm is obtained.

37/3,AB/24 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO

03243734
SEMICONDUCTOR DEVICE

PUB. NO.: 02-219234 [JP 2219234 A]
PUBLISHED: August 31, 1990 (19900831)
INVENTOR(s): TAKAISHI TAKESHI
APPLICANT(s): SEIKO EPSON CORP [000236] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-039731 [JP 8939731]
FILED: February 20, 1989 (19890220)
JOURNAL: Section: E, Section Number 1002, Volume 14, Number 520, Pg. 75, November 14, 1990 (19901114)

ABSTRACT

PURPOSE: To realize high speed operation by forming a base layer composed of second conductivity type compound **SiGe**(sub x) (0<x<10) composed of **silicon Si** and **germanium Ge**, on an emitter region composed of first conductivity type single crystal **silicon**, and forming a collector composed of first conductivity type **SiGe**(sub x) on the base layer.

CONSTITUTION: On an emitter layer 102 of an **N-type** single crystal **silicon** film epitaxially grown on a **silicon** substrate 101, a base layer 103 of **P-type** polycrystalline **SiGe**(sub x) (0<x<10) composed of **silicon Si** and **germanium Ge** doped with high concentration is formed by plasma CVD method, and then an insulating layer 105 is formed on the surface. After a window for forming an emitter is opened in the insulating layer 105, a collector layer 104 of **N-type** polycrystalline **SiGe**(sub x) is formed by the same way se the base layer; a collector is formed by etching; a collector electrode 106, a base electrode 107, and an emitter electrode 108 are formed. Thereby a circuit of **high** speed and **high performance** can be manufactured.

37/3,AB/25 (Item 7 from file: 347)

01898264

SEMICONDUCTOR DEVICE

PUB. NO.: 61-112364 [JP 61112364 A]
PUBLISHED: May 30, 1986 (19860530)
INVENTOR(s): MORI KAZUTAKA
MURATA JUN
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-233106 [JP 84233106]
FILED: November 07, 1984 (19841107)
JOURNAL: Section: E, Section Number 443, Volume 10, Number 293, Pg. 153, October 04, 1986 (19861004)

ABSTRACT

PURPOSE: To provide a **high performance** complemental MISFET without latch-up, by using a **P type silicon** in a **P type** semiconductor region, in which an **N type** MISFET is formed, using **N type germanium** in an **N type** semiconductor region, in which a **P type** MISFET is formed, and making the channel conductances of both parts approximately equal.

CONSTITUTION: In an **N type silicon** semiconductor substrate 1, a **P type silicon** well 2, in which **P type** impurities are selectively diffused, is provided. An N- channel **MOSFET** is formed in the well. At a part of the surface of the substrate 1, an **N type germanium** semiconductor region 9, in which **germanium** is selectively grown epitaxially, is formed. In this region 9, a P-channel **MOSFET** is formed. In this semiconductor device, rising time of the output waveform becomes as quick as the speed of a falling time. Unbalance between both times is eliminated, and a high speed **CMOS** inverter circuit can be formed.

37/3,AB/26 (Item 8 from file: 347)

DIALOG(R)File 347:JAPIO
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01848924
MANUFACTURE OF SEMICONDUCTOR DEVICE

PUB. NO.: 61-063024 [JP 61063024 A]
PUBLISHED: April 01, 1986 (19860401)
INVENTOR(s): NAKATSUKA MASAHIKO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-184801 [JP 84184801]
FILED: September 04, 1984 (19840904)
JOURNAL: Section: E, Section Number 426, Volume 10, Number 228, Pg. 84, August 08, 1986 (19860808)

ABSTRACT

PURPOSE: To activate the implanted ions on the titled semiconductor device in a **high** efficiency by **performing** a cap annealing by a method wherein, after ions are implanted on a semiconductor substrate, a heat treatment is performed in two stages, namely, at a low temperature for a long period and at a high temperature for a short period.

CONSTITUTION: After (sup 30)**Si** (sup +) ions are implanted for the purpose of forming an **n type** active layer 2 on the surface of a semiconductor GaAs substrate 1, a W(sub 3)**Si**(sub 3) layer 3 to be turned to a heat-resisting gate is formed by performing a sputtering method. The layer 3 is brought into the desired gate length by performing a plasma etching using SF(sub 6) gas, and after an SiO(sub 2) film 4 is grown in vapor phase, the side wall of a W(sub 5)**Si**(sub 3) gate 4 is coated by SiO(sub 2) films 5 and 6 by performing a reactive ion etching using CF(sub 4) gas. **n**(sup +) **type** layers 7 and 8 are obtained by implanting (sup 28)**Si** (sup +) ions. After a heat treatment is performed at 400 deg.C in a hydrogenous atmosphere for 48hr, and the layers 2, 7 and 8 are activated by performing an annealing at 800 deg.C for 20min. By performing the above-mentioned primary annealing, the generation of microcracks 9 and 10 on the gate end face can be prevented. Then, after removal of a protective layer 11, Au-**Ge**/Ni layers 12 and 13, a Ti-Au source electrode 14 and a drain electrode 15 are formed, and a GaAs **FET** is obtained.

37/3,AB/27 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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01713861
COLOR IMAGE SENSER

PUB. NO.: 60-192361 [JP 60192361 A]
PUBLISHED: September 30, 1985 (19850930)
INVENTOR(s): UCHIDA HIROYUKI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-047836 [JP 8447836]
FILED: March 13, 1984 (19840313)
JOURNAL: Section: E, Section Number 380, Volume 10, Number 35, Pg. 54, February 12, 1986 (19860212)

ABSTRACT

PURPOSE: To provide the titled senser with **high** speed **performance** and **high** resolving power without any crosstalk at all by a method wherein an amorphous semiconductor layer containing amorphous **germanium** or **germanium** is inserted between a blocking diode and a photodiode.

CONSTITUTION: An a-**Si** 41 formed by etching chromium and doping phosphorus, an i type a-**Si** 42, a **P type** a-**Si** 43 doped with boron are laminated as an individual electrode 22 on an insulating substrate 21 such as glass or substrate etc. to form a blocking diode. Next, an amorphous **germanium** 44 is deposited by glow discharge decomposing **germanium** gas. Then a **P type** a-**Si** 45, an i type a- **Si** 46 doped with boron by glow discharge decomposing silane, an **N type** a-**Si** 47 doped with phosphorus are successively laminated on the amorphous **germanium** to form a photodiode. Through these procedures, a color image sensor provided with **high** speed **performance** and **high** resolving power without any crosstalk at all may be produced.

37/3,AB/28 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO

01485576
MANUFACTURE OF JUNCTION GATE FIELD-EFFECT TRANSISTOR

PUB. NO.: 59-197176 [JP 59197176 A]
PUBLISHED: November 08, 1984 (19841108)
INVENTOR(s): OHATA KEIICHI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-071070 [JP 8371070]
FILED: April 22, 1983 (19830422)
JOURNAL: Section: E, Section Number 302, Volume 09, Number 56, Pg. 137, March 12, 1985 (19850312)

ABSTRACT

PURPOSE: To easily obtain an **FET**, which operates at high speed in a short gate structure, by a method wherein a high-resistance layer, which constitutes one part of a high- resistance substrate, is grown on a semiinsulative substrate, the layer is covered with a nitride film having an aperture, a groove is bored in the **high**-resistance layer by **performing** an etching, the groove is filled with a channel layer and a semiconductor layer and a gate electrode is provided thereon.

CONSTITUTION: A high-resistance GaAs layer 21, which constitutes one part of a high- resistance substrate, is deposited on a semiinsulative GaAs substrate and an **N**(sup +) **type** GaAs layer 22 is epitaxially grown thereon. Then, an **Si**(sub 3)N(sub 4) film 23 is coated on the whole surface according to a plasma CVD method, the film 23 and then the layer 22 are vertically removed by performing a reactive ion etching to obtain a gate aperture and an **N type** channel layer 24 and a **P type** GaAs layer 25, both of polycrystalline **Si**, are laminatedly formed in the aperture. After that, the surface of an polycrystalline **Si** layer 24' coated to the circumferential edge of the aperture is similarly covered with an polycrystalline **Si** layer 25' and a CrAu gate electrode 26 is coated while the upper part on the layer 25 is being filled. Then, the film 23 and the layers 24' and 25' in the circumference thereof are removed, and a source electrode 27 and a

drain electrode 28, both consisting of Au-**Ge**, are coated on the exposed layer 22.

37/3,AB/29 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO

01320574
MANUFACTURE OF FIELD EFFECT TRANSISTOR

PUB. NO.: 59-032174 [JP 59032174 A]
PUBLISHED: February 21, 1984 (19840221)
INVENTOR(s): TSUKURIDA YASUTAMI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-141934 [JP 82141934]
FILED: August 16, 1982 (19820816)
JOURNAL: Section: E, Section Number 248, Volume 08, Number 119, Pg. 50, June 05, 1984 (19840605)

ABSTRACT

PURPOSE: To obtain an **FET** with a compound semiconductor by preveinting the deterioration in the characteristics due to a reaction between a metal and the semiconductor by the application of a self-aligning method due to an ion implantation and a heat treatment by employing a junction type **FET** configuration.

CONSTITUTION: An i type GaAs active layer 22(sub 1), an **n type** GaAlAs layer 22(sub 2) and a **p type** GaAlAs layer 23 are laminated by an electron beam epitaxial method on a semi-insulating GaAs substrate 21. This estructure is etched to the vicinity of the layer 22(sub 1) with a gate region as a mask 24, **Si** ions are then implanted, the structure is heat treated, and **n type** source 25 and drain 26 are formed. Then, a CVD SiO(sub 2) film 27 is covered, a window is opened, and ohmic Au-**Ge** electrodes 28-30 are formed. The current of channel 22 can be controlled by applying negative voltage to the electrode 30 in the obtained junction type **FET**. According to this structure, a compound semiconductor is used, a self- aligning method in an **Si** gate **MOSFET** is applied, and an **FET** which has **high** density and **high performance** can be formed.

37/3,AB/30 (Item 12 from file: 347)
DIALOG(R)File 347:JAPIO

01320573
MANUFACTURE OF FIELD EFFECT TRANSISTOR

PUB. NO.: 59-032173 [JP 59032173 A]
PUBLISHED: February 21, 1984 (19840221)
INVENTOR(s): TSUKURIDA YASUTAMI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 57-141933 [JP 82141933]
FILED: August 16, 1982 (19820816)
JOURNAL: Section: E, Section Number 248, Volume 08, Number 119, Pg. 49, June 05, 1984 (19840605)

ABSTRACT

PURPOSE: To obtain an **FET** which employs a compound semiconductor without variation in the characteristics due to a reaction between a metal and the semiconductor even by a self-aligning method due to an ion implantation and a heat treatment by employing an MISFET which uses as a gate electrode the semiconductor.

CONSTITUTION: An i-type GaAs active layer 22(sub 1), an **n type** GaAlAs layer 22(sub 2), a semi-insulating GaAlAs layer 23, and an **n type** GaAs layer 24 are laminated by an electron beam epitaxial method on a semi-insulating GaA substrate 21. This structure is etched to the vicinity of the layer 22(sub 1) with a gate region as a mask 25. Then, **Si** ions are implanted, the structure is then heat treated so as to form **n type** source 26 and drain 27. The mask 25 is removed, a CVD SiO(sub 2) film 28 is covered, a hole is opened, and ohmic Au-**Ge** electrodes 29-31 are formed. The layer 24 becomes a gate electrode, the layer 23 becomes a gate insulating film, and the current of the channel 22(sub 1) can be controlled. According to this structure, a self-aligning technique in an **MOSFET** of **Si** gate is applied, and an **FET** which has **high** integration and **high performance** can be obtained with a compound semiconductor.

37/3,AB/31 (Item 13 from file: 347)
DIALOG(R)File 347:JAPIO

01015771
SEMICONDUCTOR DEVICE

PUB. NO.: 57-166071 [JP 57166071 A]
PUBLISHED: October 13, 1982 (19821013)
INVENTOR(s): OSONE TAKASHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-051476 [JP 8151476]
FILED: April 06, 1981 (19810406)
JOURNAL: Section: E, Section Number 152, Volume 07, Number 8, Pg. 34, January 13, 1983 (19830113)

ABSTRACT

PURPOSE: To obtain a **high performance C-MOS**.IC by a method wherein an N channel transistor and a P channel transistor are built in different substrates and the transistors enjoy a roughly equal mobility or the mobility ratio between the two is devised to approach the quantity one.

CONSTITUTION: An **N type Ge** substrate 22 is selectivity grown on a **P type Si** substrate 20 by the vapor deposition method. An N channel **MOS** transistor 21 is built on the substrate 20 and a P channel **MOS** transistor 23 is built on the substrate 22. Next, source regions 24 and 24' are respectively connected to a ground terminal 25 and a power source terminal 26, drain regions 27 and 27' jointly to an output terminal 29, gate electrodes 28 and 28' jointly to an output terminal 29', constituting an inverter circuit. Mobility is rough balanced between the two transistors, 1,350cm(sup 2)/V.sec for the transistor 21 and 1,900cm(sup 2)/V.sec for the transistor 23. Inductance is also roughly balanced between the two transistors and the gate oxide films can be smaller in area. Parasitic capacity decreases, which results in a high speed switching.

43/3;AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7455492 INSPEC Abstract Number: B2002-12-2570K-005
Title: Implementation of optimized **vertical** bipolar **transistor** in CMOS process technology
Author(s): Singh, U.; Singh, D.B.; Roy, J.N.
Author Affiliation: Semicond. Complex Ltd., Nagar, India
Conference Title: Proceedings of the Eleventh International Workshop on the Physics of Semiconductor Devices (SPIE Vol.4746) Part vol.1 p. 721-4 vol.1
Editor(s): Kumar, V.; Basu, P.K.
Publisher: SPIE, Washington, DC, USA
Publication Date: 2002 Country of Publication: USA 2 volume(xxxix+xl+1460) pp.
ISBN: 0 8194 4500 2 Material Identity Number: XX-2002-02457
Conference Title: Proceedings of the Eleventh International Workshop on the Physics of Semiconductor Devices
Conference Sponsor: Defence Res. & Dev. Organ.; Ministr. Inf. Technol.; Dept. Sci. & Technol.; et al
Conference Date: 11-15 Dec. 2001 Conference Location: Delhi, India
Language: English
Abstract: This paper describes the enhanced analog CMOS technology that integrates Bipolar (NPN & PNP) and CMOS on a single chip. The bipolar (both NPN and PNP) were realized using two additional mask & implant steps. For process simplicity, the P-well and the collector of PNP were formed simultaneously. The base of the PNP and NPN were made using extra **N-base** and **p-base** masking and implant steps respectively.
The **NPN transistor** with beta /sub F/ approximately=240 and BV/sub CEO/ approximately=18.0 V and the **PNP transistor** with beta /sub F/ approximately=95 and BV/sub CEO/=23.0 V were fabricated using this process technology. Commercial products have been realized using this process.
Subfile: B

43/3;AB/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014592757
WPI Acc No: 2002-413461/200244
XRAM Acc No: C02-116813
XRPX Acc No: N02-324926
Fabrication of high voltage complementary bipolar transistors in silicon-on-insulator involves forming first and second N-type and P-type sinker regions using respective first and second epitaxial silicon layers
Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: CHEN D; HEBERT F; RAZOUK R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 6365447	B1	20020402	US 985786	A	19980112	200244 B

Priority Applications (No Type Date): US 985786 A 19980112
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes

Abstract (Basic): US 6365447 B1

Abstract (Basic):

NOVELTY - High voltage complementary bipolar transistors are fabricated in a silicon-on-insulator structure by forming first N-type and P-type sinker regions and second N-type and P-type sinker regions using respective first and second epitaxial silicon layers. The N-type and P-type sinker regions are implanted with corresponding N-type and P-type dopants.

DETAILED DESCRIPTION - Fabrication of high voltage complementary **vertical NPN** and **PNP** bipolar **transistors** in a silicon-on-insulator (SOI) structure involves forming N-type buried region for the **NPN** bipolar **transistor**. The SOI structure includes a silicon substrate, a buried silicon oxide layer formed on the substrate, and a conductive silicon layer formed on the buried oxide layer. The N-type buried region is formed in the conductive silicon layer. A P-type buried region for the **PNP** bipolar **transistor** is formed in the conductive silicon layer and is spaced apart from the N-type buried region. A first epitaxial silicon layer is formed on the conductive silicon layer, and a first layer of screen silicon oxide is formed on the first epitaxial silicon layer. The first screen silicon oxide layer is masked to define spaced-apart first N-type and first P-type sinker regions in the first epitaxial silicon layer. A N-type dopant is implanted into the first N-type sinker region located above, but spaced apart from, the N-type buried **region**. A **P**-type dopant is implanted into the first P-type sinker region located above, but spaced apart from, the P-type buried region. A second epitaxial silicon layer is formed, and a second layer of screen silicon oxide is formed on the second epitaxial silicon layer. The second screen silicon oxide layer is masked to define spaced-apart second N-type and second P-type sinker regions in the second epitaxial layer. A N-type dopant is implanted into the second N-type sinker region located above, but spaced apart from, the first N-type sinker **region**. A **P**-type dopant is implanted into the second P-type sinker region located above, but spaced apart from, the first P-type sinker region. An anneal step is then performed such that N-type dopant diffuses so that the second N-type sinker region overlaps with the first N-type sinker region and the first N-type sinker region overlaps with the N-type buried region. The anneal step also allows the P-type dopant to diffuse such that the second P-type sinker region is overlaps with the first P-type sinker region and the first P-type sinker region overlaps with the P-type buried **region**. A **P** -type dopant is then implanted into the second epitaxial silicon layer to define a P-type well above the P-type buried region. An insulating trench is formed between the N-type buried region and the P-type buried region. The insulating trench extends from an upper surface at the second epitaxial silicon layer to the buried silicon oxide layer.

USE - For fabricating complementary bipolar and bi-complementary metal oxide semiconductor (**BiCMOS**) transistors.

ADVANTAGE - The use of the two epitaxial silicon layers minimizes thermal budget and therefore the up diffusion of the dopants in the NPN and PNP buried layers. Because the sinker regions are formed by diffusion of dopants at the interface of the two epitaxial layers, the dopants have a shorter distance which they must diffuse over as compared when to the situation in which they are implanted into the top surface of the of a single, thicker epitaxial layer. Thus, a shorter anneal time is required to form the sinker regions.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view illustrating high voltage complementary bipolar and **BiCMOS**

devices.
pp; 11 DwgNo 2/4

43/3,AB/3 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011973132
WPI Acc No: 1998-390042/199834
XRPX Acc No: N98-304280
Vertical PNP transistor structure for bipolar or **BiCMOS** circuit used in e.g. mobile radio or data link - comprises buried P-doped area as collector, N-doped area as **base**, and **P** -doped area as emitter, whereby P-doped polysilicon layer serves as emitter contact and base contact is, at least partially, arranged above emitter contact
Patent Assignee: SIEMENS AG (SIEI)
Inventor: BIANCO M; LACHNER R
Number of Countries: 027 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 855747	A1	19980729	EP 98100638	A	19980115	199834	B
DE 19702320	A1	19980730	DE 1002320	A	19970123	199836	
JP 10214846	A	19980811	JP 9823911	A	19980121	199842	
KR 98070685	A	19981026	KR 981813	A	19980122	199953	
TW 373334	A	19991101	TW 97120049	A	19971231	200036	

Priority Applications (No Type Date): DE 1002320 A 19970123
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 855747	A1	G	11	H01L-029/423	
	Designated States (Regional): AL AT BE CH DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI				
DE 19702320	A1			H01L-029/732	
JP 10214846	A		6	H01L-021/331	
KR 98070685	A			H01L-029/74	
TW 373334	A			H01L-029/732	

Abstract (Basic): EP 855747 A
The transistor structure includes a semiconductor substrate (1) with a buried P-doped area as a collector (2), an N-doped area as a base (5), and a base contact (10) arranged on the substrate surface. A P-doped area is formed as an emitter (9), and a P-doped poly-silicon layer on the substrate surface serves as an emitter contact (6).
The base contact is, at least partially, arranged above the emitter contact. The base contact is preferably formed of N-doped polysilicon, and the emitter contact is preferably formed as a ring around the base contact, or as a strip adjacent to the base contact.
USE - For manufacture of, especially analog, semiconductor in **BiCMOS** technology.
ADVANTAGE - Enables simplified manufacture, especially without significantly increasing complexity if transistor is integrated with corresponding **NPN transistor** structure. Has higher operation frequency due to reduced base width and reduced surface requirement. In situ doped polysilicon has better properties, especially offering very small emitter window as used for high frequency applications. Improved diffusion properties.
Dwg.1/4

43/3,AB/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011133590
WPI Acc No: 1997-111514/199711
XRPX Acc No: N97-092271
BiCMOS integrated circuit - has silicon monocrystalline substrate in which buried N, N+ and **P+** type **regions** are obtained by arsenic and boron ion implantation and diffusion while **NPN transistors** are obtained by high dose arsenic implantation and annealing
Patent Assignee: MOTOROLA SEMICONDUCTEURS SA (MOTI)
Inventor: COMBES M; FOERSTNER J; HAUTEKIET G; MARTY B A
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2736209	A1	19970103	FR 957906	A	19950630	199711	B
JP 9036249	A	19970207	JP 96212215	A	19960701	199716	

Priority Applications (No Type Date): FR 957906 A 19950630
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2736209	A1		22	H01L-027/07	
JP 9036249	A		10	H01L-021/8238	

Abstract (Basic): FR 2736209 A
The IC includes a monocrystalline silicon p type substrate (1) on which two N type buried regions are formed by arsenic ion implantation through a masking layer.
P+ type **regions** are obtained by boron ion implantation through a second masking layer (24). The diffusion of arsenic and boron ions at relatively high temperatures generates the buried **regions N-**, **N+**, and P+. The collector and emitter of **NPN transistors** and the source and drain of NMOS transistors are obtained by high dose ion implantation. an annealing process at 1020 degrees Celsius in nitrogen atmosphere is then carried out.
ADVANTAGE - Can includes **vertical PNP transistors** and active devices. Can easily include resistors, capacitors and other passive devices. Bipolar and MOS devices are integrated using single manufacturing process.
Dwg.23/25

43/3,AB/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009423291
WPI Acc No: 1993-116806/199314
XRAM Acc No: C93-051864
XRPX Acc No: N93-089074
BICMOS device mfr. having an **extrinsic base** of reduced resistance - in which emitter and **vertical PNP transistor** by using base electrode polysilicon layer as diffusion source
Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: KIM M H; WON T Y; YOO J H; YOO K D
Number of Countries: 003 Number of Patents: 003

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5196356	A	19930323	US 92874612	A	19920427	199314	B
JP 5218314	A	19930827	JP 92251164	A	19920921	199339	
KR 9407466	B1	19940818	KR 9120269	A	19911114	199622	

Priority Applications (No Type Date): KR 9120269 A 19911114

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5196356	A		8	H01L-021/265	
JP 5218314	A		6	H01L-027/06	
KR 9407466	B1			H01L-027/06	

Abstract (Basic): US 5196356 A

Mfg. **BiCMOS** devices includes (1) forming an N-type buried layer (2) in a P-type Si substrate (1) and forming a highly doped P-type bottom layer (3) and a highly doped N-type bottom layer (4); (2) growing an intrinsic epitaxial layer; (3) forming N type(5) and P type (6) wells in the epitaxial layer by a twin well process; (4) forming a channel-stop region (7) for preventing field inversion, (5) forming selectively a 1st insulating layer (11) by local oxidation of Si, (6) growing a gate oxide layer (21) and depositing a polysilicon layer (23); (7) removing first polysilicon layer (23) and gate oxide layer (21) on **NPN transistor** region (41) and **vertical PNP transistor** region (43) defined photolithographically; (8) depositing a second polysilicon layer (45) and doping with highly doped N-type impurities; (9) depositing a second insulating layer (47); (10) forming gates (53,51) of PMOS and NMOS transistors, emitter electrodes (55) and collector electrodes (57) of **NPN transistor**, and base electrodes (59) of **vertical PNP transistor** by removing predetermined parts of second insulating layer (47) and second polysilicon layer (45) photo-lithographically; (11) depositing third insulating layer and forming sidewall spacers (79) by reactive ion etching; (12) highly doping the source/drain regions of PMOS transistor, the emitter/collector regions of the **vertical PNP transistor**, and the base of **NPN transistor**; (13) removing second insulating layer (47); and (14) forming **extrinsic base** (87) of **vertical PNP transistor** by using second polysilicon layer (45) as a diffusion source.

USE/ADVANTAGE - The process is simplified and the resistance of the **extrinsic base** is reduced.

Dwg.1/20

43/3,AB/6 (Item 5 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009375409

WPI Acc No: 1993-068887/199309

XRAM Acc No: C93-030533

XRPX Acc No: N93-052877

Forming **vertical PNP transistor** in complementary **BICMOS** with EEPROM - using two dopants and giving high performance transistors with modular combinations

Patent Assignee: EXAR CORP (EXAR-N)

Inventor: AKKAN O L; ICEL A B

Number of Countries: 009 Number of Patents: 005

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 529860	A2	19930303	EP 92307301	A	19920810	199309	B
TW 200597	A	19930221	TW 92106132	A	19920803	199329	
US 5248624	A	19930928	US 91749076	A	19910823	199340	
JP 5243584	A	19930921	JP 92222668	A	19920821	199342	
EP 529860	A3	19931118	EP 92307301	A	19920810	199512	

Priority Applications (No Type Date): US 91749076 A 19910823

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 529860	A2	E	12	H01L-021/82	
Designated States (Regional): AT DE FR GB IT NL					
US 5248624	A		11	H01L-021/331	
JP 5243584	A		12	H01L-029/788	
TW 200597	A			H01L-021/205	
EP 529860	A3			H01L-021/82	

Abstract (Basic): EP 529860 A

Forming a **vertical PNP transistor** on a P substrate, in a complementary **bicmos** process with EEPROM memory, comprises forming an N buried layer (12) in the P substrate (11), forming a P buried layer in the N layer, growing a P epitaxial layer (10) over the buried layers and implanting an **N base** (13) over the P buried layer. A **P region** is then implanted (14) in the **N base** and EEPROM transistors are then formed.

Also claimed is a **vertical PNP transistor** as above, additionally comprising a perimeter N+ buried layer around the N- buried layer and a perimeter **N+** sinker **region** extending down to the N+ buried layer, with both the N+ and **N-regions** formed with As.

Pref. a field oxidation layer is formed after the transistor bases to give high-voltage transistors or pref. formed before the bases to give low-voltage transistors. Pref. N+ implants form a low resistance **extrinsic base** and NMOS source and drain; pref. P+ implants form a contact region for the PNP collector and source and drain form the PMOS.

USE/ADVANTAGE - Useful for EEPROM memories in a complementary **BICMOS** process, logic and analogue circuits. High performance vertical PNPs are provided, only two dopant species are needed, high collector to isolation breakdown voltage and low isolation layer resistivity are achieved, and different types of transistor may be integrated on the same substrate in a modular process.

Dwg.1a,1b/4

Abstract (Equivalent): US 5248624 A

Method comprises (a) forming an N-buried layer in the P substrate, (b) forming a P-buried layer in the N-buried layer, (c) growing a P-epitaxial layer over the buried layers, (d) implanting an **N-base region** over the P-buried layer, (e) implanting a **P-region** in the **N-base region**, and (f) forming EEPROM transistors after formation of the buried layers and the P-epitaxial layer. The **N-base** for the **PNP transistor** and a **P-base** for an **NPN transistor** are formed before the formation of a field oxidation layer. An **N+ region** is formed by ion implantation into the N-base region to form a low resistance **extrinsic base region** and form source and drain regions for NMOS transistors.

USE/ADVANTAGE - Used for forming a **vertical PNP transistor** on a P substrate, partic. in **BICMOS** or bipolar

technologies. Good flexibility, performance and variety of devices on the same substrate.
Dwg.3/4

43/3,AB/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008800548
WPI Acc No: 1991-304560/199142
XRPX Acc No: N91-233338
Vertical isolated-collector **PNP transistor** structure - has P-well **region** enclosed in N type pocket comprised of N plus buried layer and N reach-through region
Patent Assignee: IBM CORP (IBMC); INT BUSINESS MACHINES CORP (IBMC)
Inventor: BONNEAU D; COMBES M; DALLY A; MOLLIER P; OGURA S; TANNHOF P; DALLY A J
Number of Countries: 005 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 451423	A	19911016	EP 90480056	A	19900410	199142	B
US 5155572	A	19921013	US 91680490	A	19910404	199244	
JP 5041487	A	19930219	JP 9143721	A	19910308	199312	

Priority Applications (No Type Date): EP 90480056 A 19900410
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 451423	A				
Designated States (Regional): DE FR GB					
US 5155572	A		10	H01L-027/02	
JP 5041487	A			H01L-027/06	

Abstract (Basic): EP 451423 A
The **vertical** isolated-collector **PNP transistor** structure (58) comprises a **P+ region** (45), an **N region** (44) and a **P-** well **region** (46) forming respectively the emitter, the base and the collector of the **PNP transistor** structure. The **P-** well **region** is enclosed in a N type pocket comprised of a N+ buried layer (48) and a N reach-through region (47). The contact regions (46-1,47-1) to the **P-** well **region** and to the N reach-through region are shorted to define a common collector contact (59).
In addition, the thickness W of the **P-well region** is so minimised to allow transistor action of the parasitic **NPN transistor** formed by **N PNP base region**, **P-** well **region** and the N+ buried layer, respectively as the collector, the base and the emitter of said **PNP transistor**.
ADVANTAGE - High performance **vertical PNP transistor** with isolated collector. (12pp Dwg.No.8,9A/9)+
Abstract (Equivalent): US 5155572 A
The **vertical** isolated-collector **PNP transistor** structure comprises a **P+ region** (45), a **N region** (44) and a **P-** well **region** (46) which form the emitter, the base and the collector, respectively. The **P-** well **region** is enclosed in a N type pocket comprised of a N+ buried layer (48) in contact with a N reach-through region (47). The contact regions (46-1,47-1) to the **P-** well **region** (46) and to the N reach-through region (47) are shorted to define a common collector contact (59).

In addition, the thickness W of the **P-** well **region** (46) is minimised to allow transistor action of the parasitic **NPN transistor** formed by **N PNP base region** (44), **P-** well **region** (46) and the N+ buried layer, (48) respectively as the collector, the base and the emitter of said **PNP transistor**. The **PNP transistor** structure may be combined with a conventional **NPN transistor** structure.

USE - **BiCMOS** circuit output stage consisting of complementary bipolar transistors. Mfg. process compatible with **NPN transistor** mfr..

Dwg.4/9

43/3,AB/8 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008455962
WPI Acc No: 1990-342962/199046
XRAM Acc No: C90-148658
XRPX Acc No: N90-262279
Bismuth-CMOS IC - includes **PNP transistor** in which collector is formed in epitaxial layer and base straddles collector and epitaxial region
Patent Assignee: NEC CORP (NIDE)
Inventor: OHKI M
Number of Countries: 005 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 396948	A	19901114	EP 90107572	A	19900420	199046 B
JP 3048458	A	19910301	JP 90104969	A	19900420	199115
US 5045912	A	19910903	US 90513463	A	19900423	199138
EP 396948	B1	19971229	EP 90107572	A	19900420	199805
DE 69031846	E	19980205	DE 631846	A	19900420	199811
			EP 90107572	A	19900420	

Priority Applications (No Type Date): JP 89102427 A 19890421; JP 90104969 A 19900420
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 396948	A		10		
Designated States (Regional): DE FR GB					
US 5045912	A		8		
EP 396948	B1	E	8	H01L-027/06	
Designated States (Regional): DE FR GB					
DE 69031846	E			H01L-027/06	Based on patent EP 396948

Abstract (Basic): EP 396948 A

In an IC having **pnp** and **npn transistors** and p and a channel MOSFETs on the same substrate, the **pnp transistor** comprises: a semiconductor layer formed on the substrate; a collector layer formed on the semiconductor layer; a base layer straddling the collector and semiconductor layers; and an emitter layer on the base layer. The substrate is pref. a p-Si substrate, the **pnp transistor** being formed on an n-epitaxial layer.

ADVANTAGE - A Bi-CMOS IC is provided capable of high speed operation and a large current drive. (10pp DWg.No.2f/2

Abstract (Equivalent): EP 396948 B

In an IC having **pnp** and **npn transistors** and p and

á"channel MOSFETs on the same substrate, the **pnp transistor** comprises: a semiconductor layer formed on the substrate; a collector layer formed on the semiconductor layer; a base layer straddling the collector and semiconductor layers; and an emitter layer on the base layer. The substrate is pref. a p-Si substrate, the **pnp transistor** being formed on an n-epitaxial layer.

ADVANTAGE - A Bi-CMOS IC is provided capable of high speed operation and a large current drive.

Dwg.2a/2f

Abstract (Equivalent): US 5045912 A

Integrated circuit comprises **PNP transistor** formed on semiconductor substrate, **NPN transistor**, N-channel FET on substrate, and p-channel FET on substrate. **PNP transistor** comprises (i) N-type **base** region including two portions, first formed on substrate, second selectively formed in first portion with higher impurity concentration; (ii) P-type collector region, having specific impurity concentration range, with side surface portion contacting side surface portion of second portion of base region to form PN junction; and (iii) P-type emitter region having side surface forming PN junction with second portion along with side surface or second portion, with part of second portion of base sandwiched between side surfaces of emitter and collector regions, to form active base through which current flows. USE - For **BiCMOS** integrated circuit which monolithically integrates **vertical NPN** bipolar **transistor**, **PNP** bipolar **transistor**, N-MOSFET and P-MOSFET.

(8pp

43/3,AB/9 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO

03532035
MANUFACTURE OF **VERTICAL PNP TRANSISTOR**

PUB. NO.: 03-194935 [JP 3194935 A]
PUBLISHED: August 26, 1991 (19910826)
INVENTOR(s): HORIUCHI HITOSHI
SATOU MINAKO
APPLICANT(s): YOKOGAWA ELECTRIC CORP [000650] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-334071 [JP 89334071]
FILED: December 22, 1989 (19891222)
JOURNAL: Section: E, Section Number 1135, Volume 15, Number 454, Pg. 64, November 19, 1991 (19911119)

ABSTRACT

PURPOSE: To form a **vertical** type **PNP transistor** in an IC without complicating a process, by applying a part of process forming an **NPN transistor** and an MOSFET in a **BiCMOS** process.

CONSTITUTION: In a **BiCMOS** process, a buried layer 2 of an **NPN transistor** and a **vertical PNP transistor** is simultaneously formed on a P-type substrate 1, and an epitaxial layer 3 of N-type low concentration is grown at the same time on the buried layer 2. Next, the **P-well region** of an N-channel MOSFET is formed, and at the same time, a **P-well region** 9 is formed in the epitaxial layer 3 of the **vertical PNP transistor**. N-type diffusion is performed in the **P-well region** 9, thereby forming an

intrinsic base region 10 of the vertical type PNP transistor . By P(sup +) diffusion, the source and the drain of the P-channel MOSFET are formed, and at the same time, the emitter 11 of the vertical PNP transistor is formed in the intrinsic base region 10. A collector leading-out region 12 is formd in the P-well region 9.

43/3,AB/10 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO

02787144
BICMOS INTEGRATED CIRCUIT

PUB. NO.: 01-084744 [JP 1084744 A]
PUBLISHED: March 30, 1989 (19890330)
INVENTOR(s): HAMADA MITSUHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-244516 [JP 87244516]
FILED: September 28, 1987 (19870928)
JOURNAL: Section: E, Section Number 788, Volume 13, Number 312, Pg. 98, July 17, 1989 (19890717)

ABSTRACT

PURPOSE: To obtain a **BiCMOS** integrated circuit having a high integration, by forming a MOS transistor where a collector is connected into a collector region of a **vertical** bipolar **transistor** which is connected to a power source terminal, a drain is connected to a base of the said bipolar transistor, and a source is connected to the power source terminal respectively.
CONSTITUTION: This element comprises: an element formation region which is provided at the surface of a semiconductor substrate p(sub 15) and is made up by an n-type semiconductor layer n(sub 17) that is dielectrically isolated from surroundings; a **vertical** type **npn transistor** Q(sub 1) consisting of the said n-type semiconductor layer n(sub 17) and containing a collector region that is connected to a power souree terminal Vcc; a p-type MOS transistor M(sub 1) consisting of a p-type impurity added region that is formed selectively at the foregoing n-type semiconductor n(sub 17) and containing a source **region p** (sub 11) that is connected to the said power source Vcc as well as a drain **region p**(sub 12) that is connected to a **base region** p(sub 13) of the said **vertical** type **pnp transistor** Q(sub 1). Thus, an integration degree is improved by installing a bipolar transistor which composes an off-buffer part of a **BiCMOS** circuit as well as a p-type MOS transistor in the same element formation region.

46/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5628367 INSPEC Abstract Number: B9708-6260-197
Title: 7-mask self-aligned **SiGe** base bipolar transistors with f/sub T/ of 80 GHz
Author(s): Tashiro, T.; Hashimoto, T.; Sato, F.; Hayashi, Y.; Tatsumi, T.
Author Affiliation: VLSI Dev. Div., NEC Corp., Sagamihara, Japan
Journal: IEICE Transactions on Electronics vol.E80-C, no.5 p.707-13
Publisher: Inst. Electron. Inf. & Commun. Eng,
Publication Date: May 1997 Country of Publication: Japan
CODEN: IELEEJ ISSN: 0916-8524
SICI: 0916-8524(199705)E80C:5L.707:MSAS;1-E
Material Identity Number: P712-97006
Language: English
Abstract: A 7-mask self-aligned **SiGe** base bipolar transistor has been newly developed. This transistor offers several advancements to a super self-aligned selectively grown **SiGe** base (SSSB) transistor which has a selectively grown **SiGe**-base layer formed by a cold-wall ultra-high vacuum (UHV) CVD system. The advancements are as follows: (1) BPSG-filled arbitrary-width trench isolation on SOI is formed by high-uniformity CMP with a hydro-chuck to reduce the number of isolation fabrication steps; (2) polysilicon-plug emitter and collector electrodes are made simultaneously using an in-situ phosphorus-doped polysilicon film to decrease the distance between emitter and collector electrodes and also to reduce the electrode fabrication steps; (3) an n/sup +/-buried collector layer is made by a high-energy phosphorus ion implantation technique to eliminate collector epitaxial growth; (4) the **germanium** profile in the neutral base region is optimized to increase the **cut-off frequency** (f/sub T/) value without increasing leakage current at the base-collector junction. In the developed transistor, a high performance of 80 GHz f/sub T/ and **mask-steps** reduction are simultaneously achieved.
Subfile: B

50/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7509031 INSPEC Abstract Number: B2003-02-2560J-032
Title: Optimization of a **SiGe**:C HBT in a BiCMOS technology for low power wireless applications
Author(s): John, J.P.; Chai, F.; Morgan, D.; Keller, T.; Kirchgessner, J. ; Reuter, R.; Rueda, H.; Teplik, J.; White, J.; Wipf, S.; Zupac, D.
Author Affiliation: Semicond. Products Sector, Motorola Inc., Tempe, AZ, USA
Conference Title: Proceedings of the 2002 Bipolar/BiCMOS Circuits and Technology Meeting (Cat. No.02CH37384) p.193-6
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2002 Country of Publication: USA 241 pp.
ISBN: 0 7803 7561 0 Material Identity Number: XX-2002-02195
U.S. Copyright Clearance Center Code: 0-7803-7561-0/02/$17.00
Conference Title: 2002 IEEE Bipolar/BICMOS Circuits and Technology Meeting
Conference Sponsor: IEEE Electron Devices Society; IEEE Solid-State Circuits Soc
Conference Date: 29 Sept.-1 Oct. 2002 Conference Location: Minneapolis, MN, USA
Language: English
Abstract: The performance enhancement of a **SiGe**:C HBT for **RF** /IF applications is described for Motorola's 0.35 mu m and 0.18 mu m BiCMOS technologies. **Cutoff frequencies** (f/sub T/) have been improved from 50 GHz to 78/84 GHz (0.35/0.18 mu m BiCMOS), with a reduction in minimum noise figure (NF) from 0.7 dB to 0.30 dB. Improvements occurred through the optimization of the intrinsic collector and **base** dopant profiles, **extrinsic** collector resistance, and device layout.
Subfile: B

50/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6490137 INSPEC Abstract Number: B2000-03-1350H-021
Title: A 0.15- mu m/73-GHz f/sub max/ **RF** BiCMOS technology using cobalt silicide ring **extrinsic-base** structure
Author(s): Suzuki, H.; Yoshida, H.; Kinoshita, Y.; Fujii, H.; Yamazaki, T.
Author Affiliation: ULSI Device Dev. Labs., NEC Corp., Kanagawa, Japan
Conference Title: 1999 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.99CH36325) p.149-50
Publisher: Japan Society Appl. Phys, Tokyo, Japan
Publication Date: 1999 Country of Publication: Japan xvi+174 pp.
ISBN: 4 930813 93 X Material Identity Number: XX-1999-02839
Conference Title: 1999 Symposium on VLSI Technology. Digest of Technical Papers
Conference Date: 14-16 June 1999 Conference Location: Kyoto, Japan
Language: English
Abstract: This paper presents an advanced **RF** mixed-signal BiCMOS technology. A single-polysilicon bipolar transistor with a high maximum frequency of oscillation (f/sub max/) is successfully implemented into a 0.15 mu m dual gate CMOS process. To achieve such a bipolar transistor, a cobalt silicide (CoSi/sub 2/) ring-shaped **extrinsic-base** structure is newly developed. This bipolar transistor demonstrates 73 GHz

f/sub max/, minimum noise figure (NF/sub min/) of 1.1 dB and a **cut-off frequency** emitter-to-collector breakdown voltage (f/sub T/.BV/sub CEO/) product of 160 GHz.V, which is competitive with previously repofted **SiGe**-based technology.
Subfile: B

50/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05804887
E.I. No: EIP00025070136
Title: 0.15- mu m/73-GHz f//m//a//x **RF** BiCMOS technology using cobalt silicide ring **extrinsic-base** structure
Author: Suzuki, Hisamitsu; Yoshida, Hiroshi; Kinoshita, Yasushi; Fujii, Hiroki; Yamazaki, Tohru
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1999 Symposium on VLSI Technology
Conference Location: Kyoto, Jpn Conference Date: 20990614-20990616
E.I. Conference Number: 56097
Source: Digest of Technical Papers - Symposium on VLSI Technology 1999. IEEE, Piscataway, NJ, USA. p 149-150
Publication Year: 1999
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: This paper presents an advanced **RF** mixed-signal BiCMOS technology. A single-polysilicon bipolar transistor with a high maximum frequency of oscillation (f//m//a//x) is successfully implemented into a 0.15 mu m dual gate CMOS process. To achieve such a bipolar transistor, a cobalt silicide (CoSi//2) ring-shaped **extrinsic-base** structure is newly developed. This bipolar transistor demonstrates 73 GHz f//m//a//x, minimum noise figure (NF//m//i//n) of 1.1 dB and a **cut-off frequency** emitter-to-collector break down voltage (f//T center dot BV//C//E//O) products of 160 GHz center dot V, which is competitive with the previously reported **SiGe**-based technology. (Author abstract) 5 Refs.

50/3,AB/4 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01911983 AADAAIC809952
High frequency characterization and modeling of **silicon germanium** heterojunction bipolar transistors
Author: Malm, B. Gunnar
Degree: Ph.D.
Year: 2002
Corporate Source/Institution: Kungliga Tekniska Hogskolan (Sweden) (1022)
Source: VOLUME 63/04-C OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 845. 95 PAGES
Publisher: Royal Institute of Technology, S-100 44 Stockholm, Sweden

High-speed, low voltage **Silicon-Germanium** (**SiGe**) heterojunction bipolar transistors (HBTs) have been designed, fabricated, electrically characterized and modeled. The **SiGe** HBTs are suitable for use in **radio frequency** (**RF**) integrated circuit (IC)

applications and were fabricated using non-selective epitaxial growth. The design of the **extrinsic base region** has been investigated in detail. Transient enhanced diffusion of boron, caused by the **extrinsic base** implantation, was found to degrade DC and high-frequency electrical characteristics. It was also found that the low-frequency noise was affected by the base design. Furthermore, a hydrogen anneal was found to reduce the low-frequency noise in polysilicon emitter bipolar transistors. The high-frequency noise of **SiGe** HBTs was investigated experimentally as well as by device simulation. Noise parameter extraction methods based on direct admittance or Y-parameter measurement have been investigated in detail. Good agreement was found with conventional noise figure measurement. **SiGe** HBTs were fabricated to investigate the optimization of ion-implanted collector doping profiles. A novel concept was suggested where a low-energy (5–10 keV) antimony (Sb) implantation was combined with a standard selectively implanted collector (SIC) using phosphorous. Segregation of Sb was found to occur during the subsequent growth of the epitaxial **SiGe** base layer. The resulting broadening of the implanted Sb-profile degraded the DC-electrical characteristics of the device. The devices with an Sb-implantation exhibited a **cut-off frequency** of more than 60 GHz. A mixed-mode circuit and device simulation methodology was developed to investigate the **RF** harmonic distortion of **SiGe** HBTs. The influence on harmonic distortion of the **Ge**-profile as well as the collector doping profile was quantified. High-injection heterojunction barrier effects due to the presence of a valence band offset at the base-collector junction were found to significantly affect the harmonic distortion. Devices with a **Ge**-profile retrograded towards the collector exhibited significantly reduced harmonic distortion. Increasing the **Ge**-concentration at the base-emitter junction led to reduced harmonic distortion for low current operation. A non-uniform collector doping profile was shown to suppress the harmonic distortion and increase the breakdown voltage.